ES29LV160F

16 Megabit (2 M x 8-Bit/1 M x 16-Bit)
CMOS 3.0 Volt-only Boot Sector Flash Memory

Excel Semiconductor inc.

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Main Characteristics

Architectural Advantages

- **Single Power Supply Operation**
  - Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
- **Flexible Sector Architecture**
  - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
  - One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
- **Sector Protection Features**
  - A hardware method of locking a sector to prevent any program or erase operations within that sector
  - Sectors can be locked in-system or via programming equipment
  - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Top or Bottom Boot Block Configurations Available**
- **Compatibility with JEDEC standards**
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection

Performance Characteristics

- **High Performance**
  - Access times as fast as 55ns
  - Commercial (0°C to +70°C) and Industrial temperature range (-40°C to +85°C)
- **Program and erase performance (typical values)**
  - Program time, 5us/byte, 7us/word
  - Erase time 0.4sec/sector
- **Ultra Low Power Consumption (typical values)**
  - 10uA Automatic Sleep mode current
  - 10uA standby mode current
  - 9 mA read current at 5MHz
  - 15 mA program/erase current
- **Cycling Endurance: Minimum 100,000 cycles per sector**
- **Data Retention: 20 years typical**

Package Options

- **48-ball FBGA (6 mm x 8 mm)**
- **48-pin TSOP**

Software & Hardware Features

- **CFI (Common Flash Interface) Compliant**
  – Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Erase Suspend/Erase Resume**
  – Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Data# Polling and Toggle Bits**
  – Provides a software method of detecting program or erase operation completion
- **Ready/Busy# Pin (RY/BY#)**
  – Provides a hardware method of detecting program or erase cycle completion
- **Hardware Reset Pin (RESET#)**
  – Hardware method to reset the device to reading array data

Additional Features

In ES29LV160F device, a few of additional and useful features are provided. These are additional so that its functionality is 100% compatible with other flash devices. More and detail explanations for each additional features can be found at page 58.

- Deep power-down mode (less than 1uA)
- Program acceleration mode by ACC pin, effectively 4usec/word
- Page buffer program (32 words), effectively 5usec/word
- Page buffer program with ACC pin acceleration, effectively 2usec/word
- 256 bytes of security sector for customer codes
- Factory and customer-lockable functions for the security sector

General Description

The ES29LV160F is a 16Mbit, 3.0 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The device is offered in 48-ball FBGA, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in system with the standard system 3.0 volt V_{CC} supply. A 12.0 V VPP or 5.0 V_{CC} are not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 55 ns and 70 ns allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The ES29LV160F is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

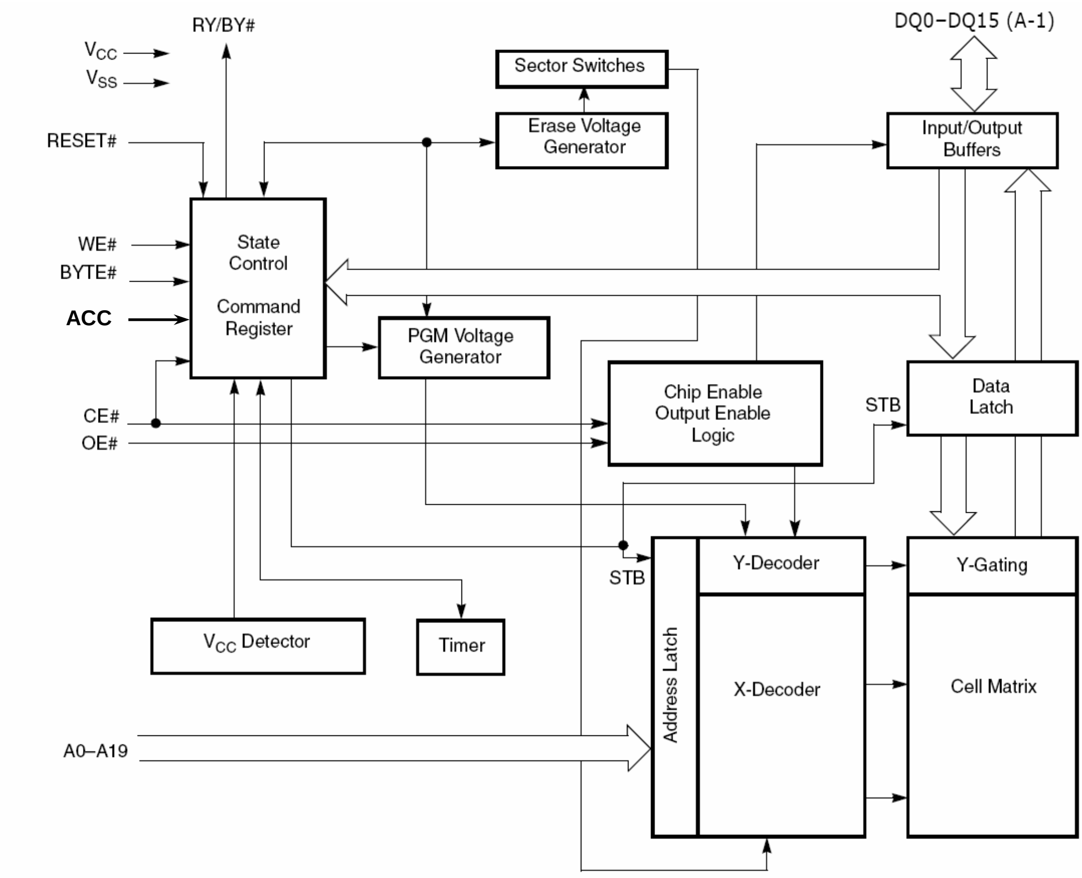
ESI's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

1. Product Selector Guide

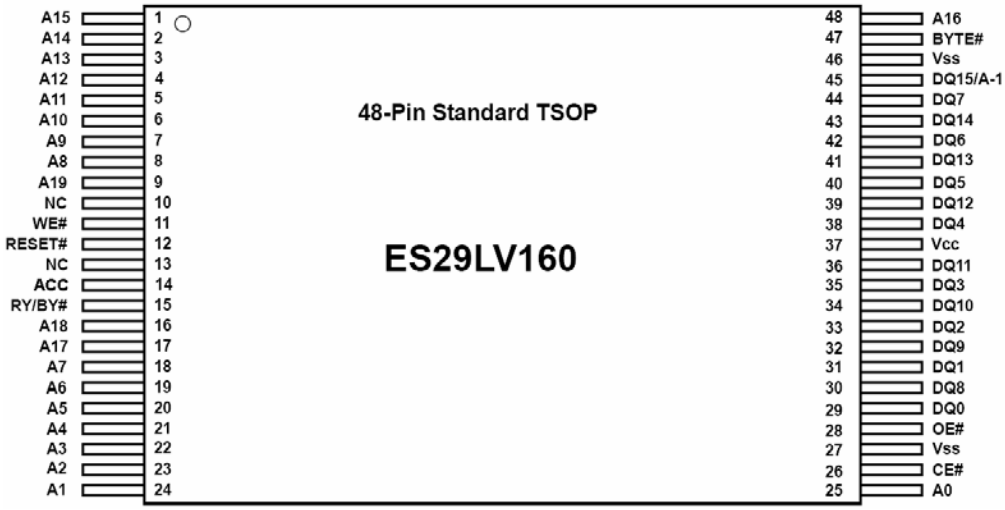
Family Part Number	ES29LV160F	
Speed Option	**55R**	**70**
Voltage Range (Vcc)	**3.0 ~3.6V**	**2.7 ~3.6V**
Max access time, ns (t_{ACC})	**55**	**70**
Max CE# access time, ns (t_{CE})	**55**	**70**
Max OE# access time, ns (t_{OE})	**25**	**30**

Note
See AC Characteristics on page 45 for full specifications.

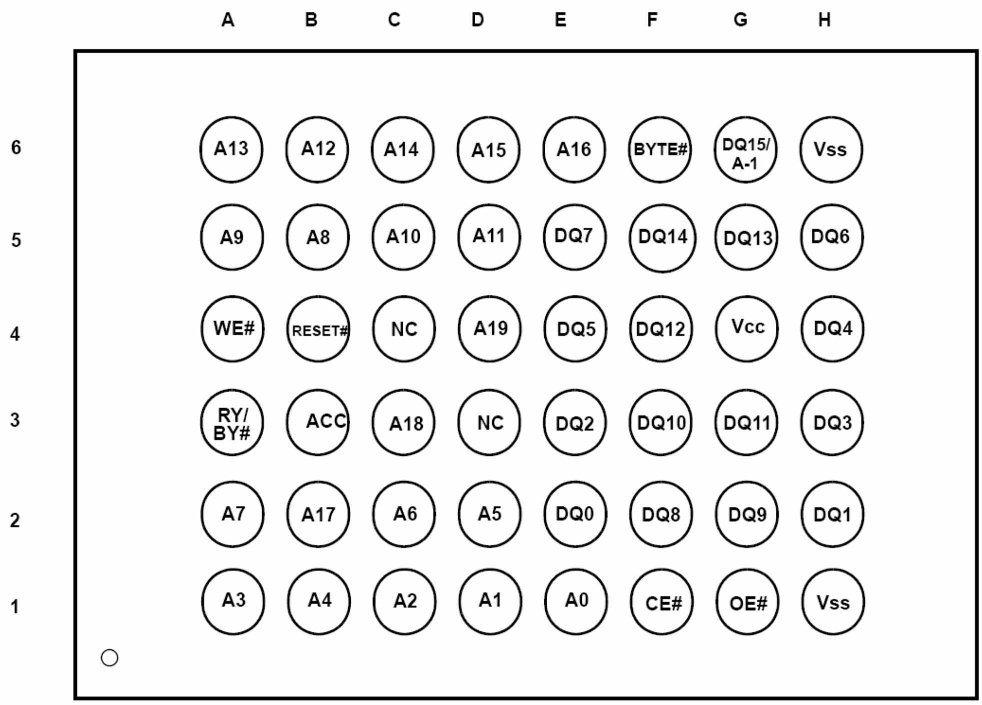
2. Block Diagram



3. Connection Diagrams



48-Ball FBGA (6 x 8 mm)
(Top View, Balls Facing Down)



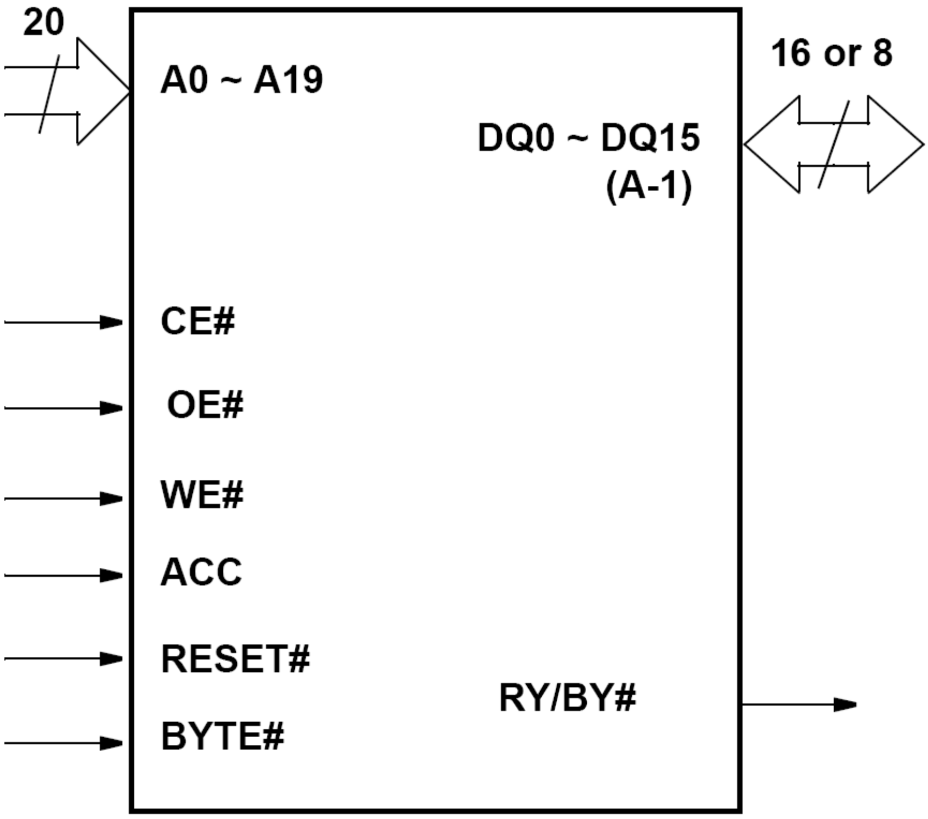
3.1 Special Handling Instructions

Special handling is required for Flash Memory products in FBGA packages.
Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4. Pin Configuration

AO-A19	20 addresses
DQ0-DQ14	15 data inputs/outputs
DQ15/A -1	DQ15 (data inputs/outputs, word mode), A-1 (LSB address input, byte mode)
BYTE#	Selects 8-bit or 16-bit mode
CE#	Chip enable
OE#	Output enable
WE#	Write enable
RESET#	Hardware reset pin
ACC	Program acceleration pin
RY/BY#	Ready/Busy output
V_{CC}	3.0 volt-only single power supply (see *Product Selector Guide on page 5* for speed options and voltage supply tolerances)
V_{SS}	Device ground
NC	Pin not connected internally

5. Logic Symbol



About ACC pin (for programming acceleration mode)

ACC pin is an extra pin to be used for an accelerated programming. Programming speed is more accelerated when 12V voltage is applied to this ACC pin. About 40% program time can be saved with this mode. However, ACC pin can be floated or non-connected (NC) if users do not want use this pin. This flexible feature is provided for full compatibility with other vendors' flash memory devices.

6. Ordering Information

ESI standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below. Valid option combinations are planned to be supported in volume. Consult your local sales office to confirm availability of specific valid combinations and check on newly released combinations.

ES 29 LV 160F X - XX X X X X

TEMPERATURE RANGE
Blank : Commercial (0℃ to +70℃)
I : Industrial (- 40℃ to +85℃)

Pb-free
C : Pb product
G : Pb-free product

PACKAGE TYPE
T: Standard TSOP (48-pin) W: FBGA(48-ball)

VOLTAGE RANGE
Blank : 2.7V ~ 3.6V
R : 3.0V ~ 3.6V

SPEED OPTION
55 : 55ns 70 : 70ns

SECTOR ARCHITECTURE
Blank : Uniform sector
T : Top Sector
B : Bottom sector

DENSITY & ORGANIZATION
400 : 4M (x8 / x16) 800 : 8M (x8 / x16)
160 : 16M (x8 / x16) 320 : 32M (x8 / x16)
640 : 64M (x8 / x16)
F : version identifier

POWER SUPPLY AND INTERFACE
F : 5.0V LV : 3.0V
DL : 3.0V, Dual Bank DS : 1.8V, Dual Bank
BDS : 1.8V, Burst mode, Dual Bank

COMPONEMT GROUP
29: Flash Memory

EXCEL SEMICONDUCTOR

7. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 7.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 7.1 ES29LV160F Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	Addresses (Note 1)	DQ0-DQ7	DQ8-DQ15	
							BYTE# $=V_{IH}$	BYTE# $=V_{IL}$
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	DQ8-DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	
Standby	$V_{CC}\pm$ 0.3 V	X	X	$V_{CC}\pm$ 0.3 V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	Sector Address, A6=L, A1=H, A0=L	D_{IN}	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend

L = Logic Low = VIL, H = Logic High = VIH, VID = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In,
D_{IN} = Data In, D_{OUT} = Data Out

Notes

1. Addresses are A19:A0 in word mode (BYTE# = VIH), A19:A-1 in byte mode (BYTE# = VIL).

2. The sector protect and sector unprotect functions may also be implemented via programming equipment. See Sector Protection/ Unprotection on page 18.

7.1 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic *1*, the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#. If the BYTE# pin is set at logic *0*, the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

7.2 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to VIL. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at VIH. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See *Reading Array Data* on page 25 for more information. Refer to the AC *Read Operations* on page 45 for timing specifications and to Figure 17.1 on page 45 for the timing diagram. ICC1 in *DC Characteristics* on page 41 represents the active current specification for reading array data.

7.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to VIL, and OE# to VIH.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. See *Word/Byte Configuration* on page 12 for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. *Word/ Byte Program Command Sequence* on page 26 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 7.2 on page 15 and Table 7.3 on page 16 indicate the address space that each sector occupies. A “sector address” consists of the address bits required to uniquely select a sector. The *Command Definitions* on page 25 has details on erasing a sector or the entire chip, or suspending/resuming the erase operation. After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to *Autoselect Mode* on page 17 and *Autoselect Command Sequence* on page 26 for more information.

ICC2 in *DC Characteristics* on page 41 represents the active current specification for the write mode. *AC Characteristics* on page 45 contains timing specification tables and timing diagrams for write operations.

7.4 Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and ICC read specifications apply. Refer to *Write Operation Status* on page 33 for more information, and to *AC Characteristics* on page 45 for timing diagrams.

7.5 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3 V. (Note that this is a more restricted voltage range than VIH.) If CE# and RESET# are held at VIH, but not within V_{CC} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (tCE) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

ICC3 represents the standby current specification shown in the table in *DC Characteristics* on page 41.

7.6 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for tACC + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. ICC5 in the *DC Characteristics* on page 41 represents the automatic sleep mode current specification.

7.7 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin to VIL for at least a period of tRP, the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at **Vss**±0.3 V, the device draws CMOS standby current (ICC4). If RESET# is held at VIL but not within **Vss**±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a *0* (busy) until the internal reset operation is complete, which requires a time of tREADY (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is *1*), the reset operation is completed within a time of tREADY (not during Embedded Algorithms). The system can read data tRH after the RESET# pin returns to VIH.

Refer to the tables in *AC Characteristics* on page 45 for RESET# parameters and to Figure 17.2 on page 46 for the timing diagram.

7.8 Output Disable Mode

When the OE# input is at VIH, output from the device is disabled. The output pins are placed in the high impedance state.

Table 7.2 Sector Address Tables (Top Boot Device)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
										Byte Mode(x8)	Word Mode(x16)
SA0	0	0	0	0	0	X	X	X	64/32	000000-00FFFF	00000-07FFF
SA1	0	0	0	0	1	X	X	X	64/32	010000-01FFFF	08000-0FFFF
SA2	0	0	0	1	0	X	X	X	64/32	020000-02FFFF	10000-17FFF
SA3	0	0	0	1	1	X	X	X	64/32	030000-03FFFF	18000-1FFFF
SA4	0	0	1	0	0	X	X	X	64/32	040000-04FFFF	20000-27FFF
SA5	0	0	1	0	1	X	X	X	64/32	050000-05FFFF	28000-2FFFF
SA6	0	0	1	1	0	X	X	X	64/32	060000-06FFFF	30000-37FFF
SA7	0	0	1	1	1	X	X	X	64/32	070000-07FFFF	38000-3FFFF
SA8	0	1	0	0	0	X	X	X	64/32	080000-08FFFF	40000-47FFF
SA9	0	1	0	0	1	X	X	X	64/32	090000-09FFFF	48000-4FFFF
SA10	0	1	0	1	0	X	X	X	64/32	0A0000-0AFFFF	50000-57FFF
SA11	0	1	0	1	1	X	X	X	64/32	0B0000-0BFFFF	58000-5FFFF
SA12	0	1	1	0	0	X	X	X	64/32	0C0000-0CFFFF	60000-67FFF
SA13	0	1	1	0	1	X	X	X	64/32	0D0000-0DFFFF	68000-6FFFF
SA14	0	1	1	1	0	X	X	X	64/32	0E0000-0EFFFF	70000-77FFF
SA15	0	1	1	1	1	X	X	X	64/32	0F0000-0FFFFF	78000-7FFFF
SA16	1	0	0	0	0	X	X	X	64/32	100000-10FFFF	80000-87FFF
SA17	1	0	0	0	1	X	X	X	64/32	110000-11FFFF	88000-8FFFF
SA18	1	0	0	1	0	X	X	X	64/32	120000-12FFFF	90000-97FFF
SA19	1	0	0	1	1	X	X	X	64/32	130000-13FFFF	98000-9FFFF
SA20	1	0	1	0	0	X	X	X	64/32	140000-14FFFF	A0000-A7FFF
SA21	1	0	1	0	1	X	X	X	64/32	150000-15FFFF	A8000-AFFFF
SA22	1	0	1	1	0	X	X	X	64/32	160000-16FFFF	B0000-B7FFF
SA23	1	0	1	1	1	X	X	X	64/32	170000-17FFFF	B8000-BFFFF
SA24	1	1	0	0	0	X	X	X	64/32	180000-18FFFF	C0000-C7FFF
SA25	1	1	0	0	1	X	X	X	64/32	190000-19FFFF	C8000-CFFFF
SA26	1	1	0	1	0	X	X	X	64/32	1A0000-1AFFFF	D0000-D7FFF
SA27	1	1	0	1	1	X	X	X	64/32	1B0000-1BFFFF	D8000-DFFFF
SA28	1	1	1	0	0	X	X	X	64/32	1C0000-1CFFFF	E0000-E7FFF
SA29	1	1	1	0	1	X	X	X	64/32	1D0000-1DFFFF	E8000-EFFFF
SA30	1	1	1	1	0	X	X	X	64/32	1E0000-1EFFFF	F0000-F7FFF
SA31	1	1	1	1	1	0	X	X	32/16	1F0000-1F7FFF	F8000-FBFFF
SA32	1	1	1	1	1	1	0	0	8/4	1F8000-1F9FFF	FC000-FCFFF
SA33	1	1	1	1	1	1	0	1	8/4	1FA000-1FBFFF	FD000-FDFFF
SA34	1	1	1	1	1	1	1	X	16/8	1FC000-1FFFFF	FE000-FFFFF
Security	1	1	1	1	1	1	1	1	256/128 (bytes/words)	1FFF00-1FFFFF	FFF80-FFFFF

Note

Address range is A19:A-1 in byte mode and A19:A0 in word mode. See Word/Byte Configuration on page 12.

Table 7.3 Sector Address Tables (Bottom Boot Device)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
										Byte Mode(x8)	Word Mode(x16)
SA0	0	0	0	0	0	0	0	X	16/8	000000-003FFF	00000-01FFF
SA1	0	0	0	0	0	0	1	0	8/4	004000-005FFF	02000-02FFF
SA2	0	0	0	0	0	0	1	1	8/4	006000-007FFF	03000-03FFF
SA3	0	0	0	0	0	1	X	X	32/16	008000-00FFFF	04000-07FFF
SA4	0	0	0	0	1	X	X	X	64/32	010000-01FFFF	08000-0FFFF
SA5	0	0	0	1	0	X	X	X	64/32	020000-02FFFF	10000-17FFF
SA6	0	0	0	1	1	X	X	X	64/32	030000-03FFFF	18000-1FFFF
SA7	0	0	1	0	0	X	X	X	64/32	040000-04FFFF	20000-27FFF
SA8	0	0	1	0	1	X	X	X	64/32	050000-05FFFF	28000-2FFFF
SA9	0	0	1	1	0	X	X	X	64/32	060000-06FFFF	30000-37FFF
SA10	0	0	1	1	1	X	X	X	64/32	070000-07FFFF	38000-3FFFF
SA11	0	1	0	0	0	X	X	X	64/32	080000-08FFFF	40000-47FFF
SA12	0	1	0	0	1	X	X	X	64/32	090000-09FFFF	48000-4FFFF
SA13	0	1	0	1	0	X	X	X	64/32	0A0000-0AFFFF	50000-57FFF
SA14	0	1	0	1	1	X	X	X	64/32	0B0000-0BFFFF	58000-5FFFF
SA15	0	1	1	0	0	X	X	X	64/32	0C0000-0CFFFF	60000-67FFF
SA16	0	1	1	0	1	X	X	X	64/32	0D0000-0DFFFF	68000-6FFFF
SA17	0	1	1	1	0	X	X	X	64/32	0E0000-0EFFFF	70000-77FFF
SA18	0	1	1	1	1	X	X	X	64/32	0F0000-0FFFFF	78000-7FFFF
SA19	1	0	0	0	0	X	X	X	64/32	100000-10FFFF	80000-87FFF
SA20	1	0	0	0	1	X	X	X	64/32	110000-11FFFF	88000-8FFFF
SA21	1	0	0	1	0	X	X	X	64/32	120000-12FFFF	90000-97FFF
SA22	1	0	0	1	1	X	X	X	64/32	130000-13FFFF	98000-9FFFF
SA23	1	0	1	0	0	X	X	X	64/32	140000-14FFFF	A0000-A7FFF
SA24	1	0	1	0	1	X	X	X	64/32	150000-15FFFF	A8000-AFFFF
SA25	1	0	1	1	0	X	X	X	64/32	160000-16FFFF	B0000-B7FFF
SA26	1	0	1	1	1	X	X	X	64/32	170000-17FFFF	B8000-BFFFF
SA27	1	1	0	0	0	X	X	X	64/32	180000-18FFFF	C0000-C7FFF
SA28	1	1	0	0	1	X	X	X	64/32	190000-19FFFF	C8000-CFFFF
SA29	1	1	0	1	0	X	X	X	64/32	1A0000-1AFFFF	D0000-D7FFF
SA30	1	1	0	1	1	X	X	X	64/32	1B0000-1BFFFF	D8000-DFFFF
SA31	1	1	1	0	0	X	X	X	64/32	1C0000-1CFFFF	E0000-E7FFF
SA32	1	1	1	0	1	X	X	X	64/32	1D0000-1DFFFF	E8000-EFFFF
SA33	1	1	1	1	0	X	X	X	64/32	1E0000-1EFFFF	F0000-F7FFF
SA34	1	1	1	1	1	X	X	X	64/32	1F0000-1FFFFF	F8000-FFFFF
Security	0	0	0	0	0	0	0	0	256/128 (bytes/words)	000000-0000FF	00000-0007F

Note

Address range is A19:A-1 in byte mode and A19:A0 in word mode. See the Word/Byte Configuration on page 12.

7.9 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires VID (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 7.4. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 7.2 on page 15 and Table 7.3 on page 16). Table 7.4 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 10.1 on page 32. This method does not require VID. See *Command Definitions* on page 25 for details on using the autoselect mode.

Table 7.4 ES29LV160F Autoselect Codes (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A19 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: ESI		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	X	**4Ah**
Device ID: ES29LV160F (Top Boot Block)	**Word**	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22h	C4h
	Byte	L	L	H										X	C4h
Device ID: ES29LV160F (Bottom Boot Block)	**Word**	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22h	49h
	Byte	L	L	H										X	49h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	01h(protected)
														X	00h(unprotected)

Legend
L = Logic Low = VIL, H = Logic High = VIH, SA = Sector Address, X = Don't care
Note
The autoselect codes may also be accessed in-system via command sequences. See Table 10.1 on page 32.

7.10 Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The device is shipped with all sectors unprotected. ESI offers the option of programming and protecting sectors at its factory prior to shipping the device through ESI's High-way™ Service. Contact a ESI representative for details.
It is possible to determine whether a sector is protected or unprotected. See *Autoselect Mode* on page 17 for details.

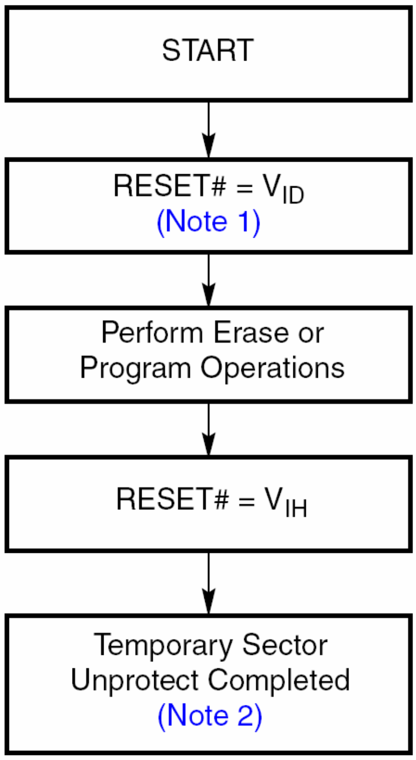
Sector protection/unprotection can be implemented via two methods.

The primary method requires VID on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 7.3 on page 20 shows the algorithms and Figure 17.12 on page 53 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

7.11 Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to VID. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once VID is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 7.2 shows the algorithm, and Figure 17.11 on page 52 shows the timing diagrams, for this feature.

Figure 7.2 Temporary Sector Unprotect Operation

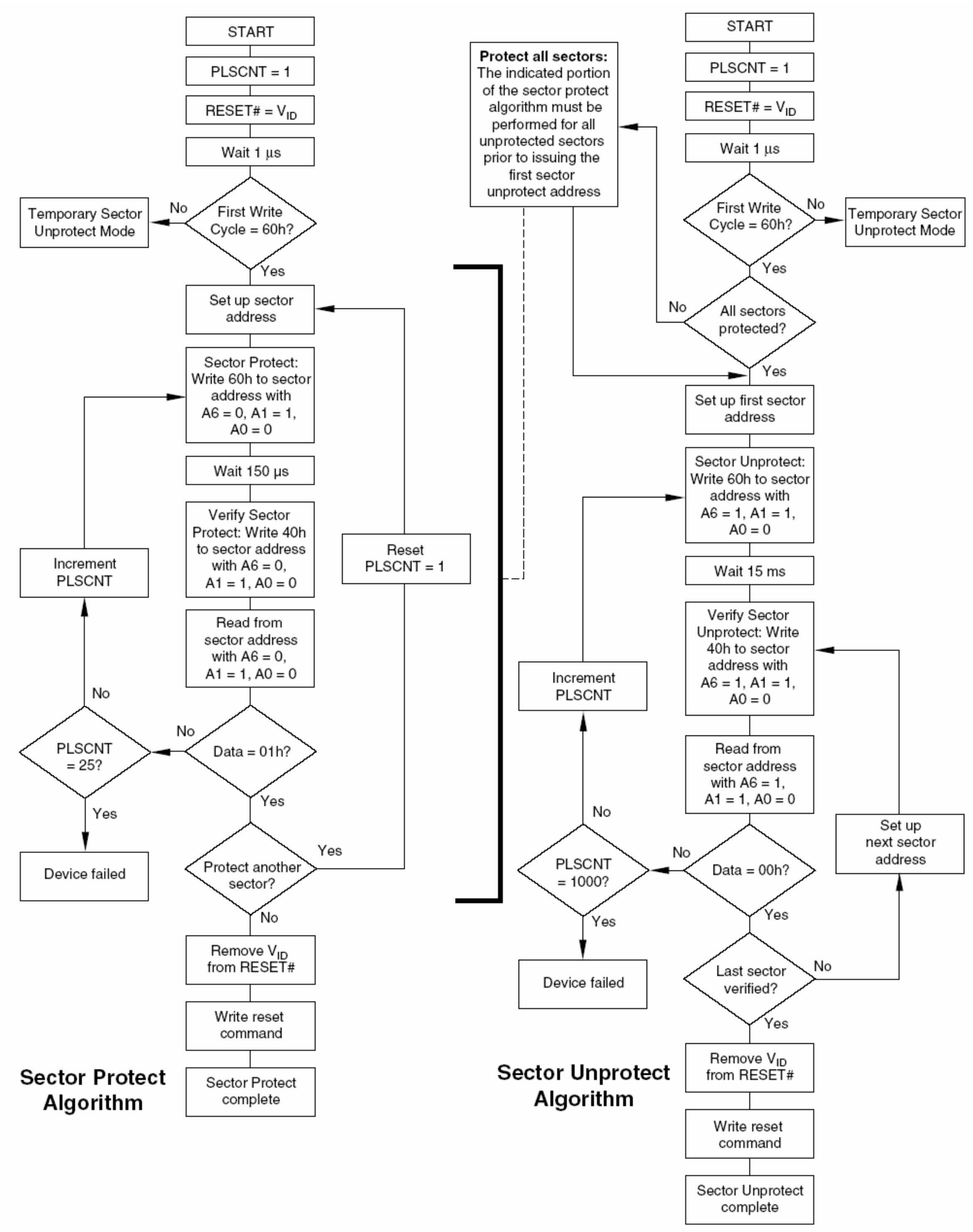


Notes

1. All protected sectors unprotected.

2. All previously protected sectors are protected once again.

Figure 7.3 In-System Sector Protect/Unprotect Algorithms



8. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 8.1 to Table 8.4 on page 21-23. In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 8.1 to Table 8.4 on page 21-23. The system must write the reset command to return the device to the autoselect mode.

Table 8.1 CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 8.2 System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7-D4: volt, D3-D0: 100 mV
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7-D4 : volt, D3-D0: 100 mV
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N us
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N us (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 8.3 Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0015h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (02h = x8,x16 Asynchronous)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0004h	Number of Erase Block Regions within device

2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0000h 0000h 0040h 0000h	Erase Block Region 1 Information (Number of identical size erase block = 0000h+1 = 1 Block size in Region 1 = 0040h*256 byte = 16 Kbyte)
31h 32h 33h 34h	62h 64h 66h 68h	0001h 0000h 0020h 0000h	Erase Block Region 2 Information (Number of identical size erase block = 0001h+1 = 2 Block size in Region 2 = 0020h*256 byte = 8 Kbyte)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0080h 0000h	Erase Block Region 3 Information (Number of identical size erase block = 0000h+1 = 1 Block size in Region 3 = 0080h*256 byte = 32 Kbyte)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	001Eh 0000h 0000h 0001h	Erase Block Region 4 Information (Number of identical size erase block = 001Eh+1 = 31 Block size in Region 4 = 0100h*256 byte = 64 Kbyte)

Table 8.4 Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string " PRI"
43h	86h	0031h	Major version number, ASCII
44h	88h	0030h	Major version number, ASCII
45h	8Ah	0000h	Address Sensitive Unlock 0 = Required, 1 = To Required
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors per group
48h	90h	0001h	Sector Temporary Unprotect 0 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect 04 = In-system Method and A9 High-Voltage Method
4Ah	94h	0000h	Simultaneous Operation 00= Not Supported, 01 = Supported

4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 =4 Word Page, 02 = Word Page
4Dh	9Ah	00B5h	ACC(Acceleration) Supply Minimum 00 = Not Supported, D7-D4: Volt, D3-D0:100mV
4Eh	9Ch	00C5h	ACC(Acceleration) Supply Maximum 00 = Not Supported, D7-D4: Volt, D3-D0:100mV
4Fh	9Eh	000xh	Top/Bottom Boot Sector Flag 3 = Top, 2 = Bottom

8.1 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 10.1 on page 32 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

8.1.1 Low V_{CC} Write Inhibit

When V_{CC} is less than VLKO, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than VLKO. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than VLKO.

8.1.2 Write Pulse Glitch Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

8.1.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = VIL, CE# = VIH or WE# = VIH. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

8.1.4 Power-Up Write Inhibit

If WE# = CE# = VIL and OE# = VIH during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

9. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 10.1 on page 32 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in *AC Characteristics* on page 45.

9.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See *Erase Suspend/ Erase Resume Commands* on page 30 for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See *Reset Command* on page 25.

See also *Requirements for Reading Array Data* on page 12 for more information. The *Read Operations* on page 45 provides the read parameters, and Figure 17.1 on page 45 shows the timing diagram.

9.2 Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don’t care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

9.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 10.1 on page 32 shows the address and data requirements. This method is an alternative to that shown in Table 7.4 on page 17, which is intended for PROM programmers and requires VID on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in word mode (or 04h in byte mode) returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table 7.2 on page 15 and Table 7.3 on page 16 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

9.4 Word/Byte Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 10.1 on page 32 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See *Write Operation Status* on page 33 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.
Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a *0* back to a *1*.** Attempting to do so may halt the operation and set DQ5 to *1*, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still *0*. Only erase operations can convert a *0* to a *1*.

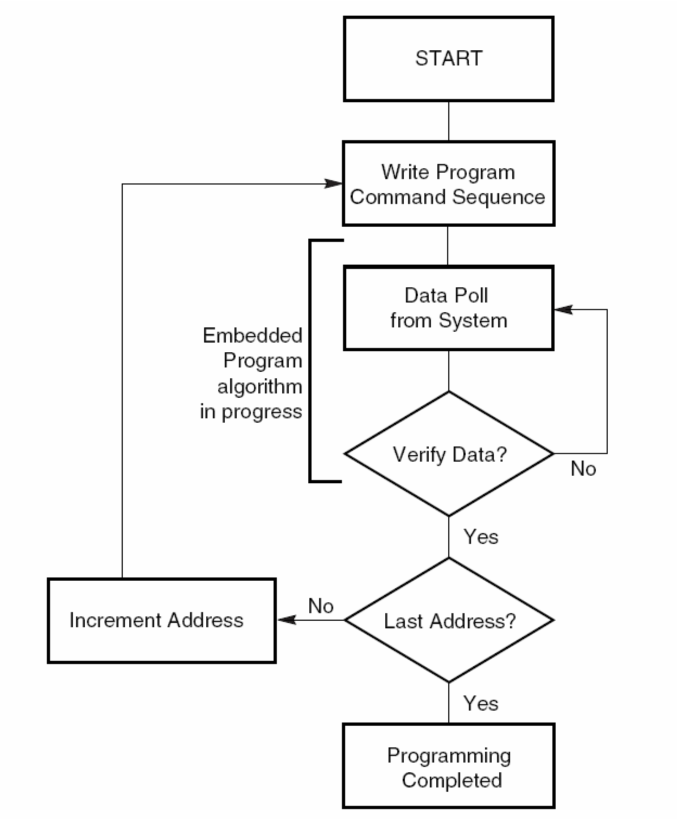
9.5 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program
command sequence, resulting in faster total programming time. Table 10.1 on page 32 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.

Figure 9.1 on page 28 illustrates the algorithm for the program operation. See *Erase/Program Operations* on page 49 for parameters, and to Figure 17.5 on page 49 for timing diagrams.

Figure 9.1 Program Operation



Note
See Table 10.1 on page 32 for program command sequence.

9.6 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 10.1 on page 32 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a

hardware reset during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See *Write Operation Status* on page 33 for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 9.2 on page 31 illustrates the algorithm for the erase operation. See *Erase/Program Operations* on page 49 for parameters, and Figure 17.6 on page 50 for timing diagrams.

9.7 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 10.1 on page 32 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See *DQ3: Sector Erase Timer* on page 38.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to *Write Operation Status* on page 33 for information on these status bits.)

Figure 9.2 on page 31 illustrates the algorithm for the erase operation. Refer to *Erase/Program Operations* on page 49 for parameters, and to Figure 17.6 on page 50 for timing diagrams.

9.8 Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are *don't-cares* when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

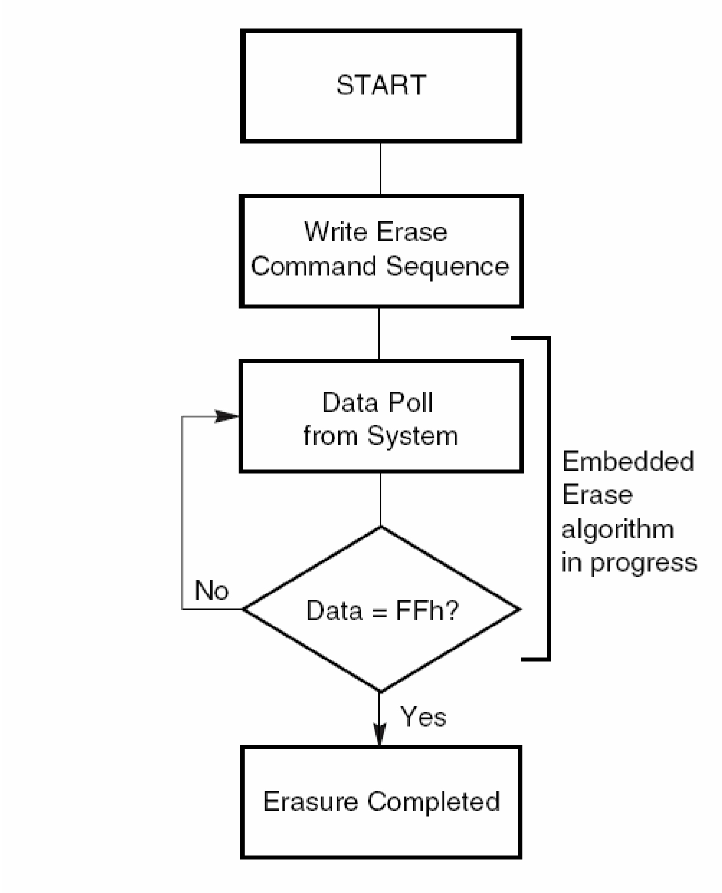
After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See *Write Operation Status* on page 33 for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See *Write Operation Status* on page 33 for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See *Autoselect Command Sequence* on page 26 for more information.

The system must write the Erase Resume command (address bits are *don't care*) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Figure 9.2 Erase Operation



Notes

1. See Table 10.1 on page 32 for erase command sequence.

2. See DQ3: Sector Erase Timer on page 38 for more information.

10. Command Definitions

Table 10.1 ES29LV160F Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2-5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	**F0**										
Autoselect (Note 8)	Manufacturer ID	Word	4	555	AA	2AA	55	555	**90**	X00	**4A**				
		Byte		AAA		555		AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	**90**	X01	22C4				
		Byte		AAA		555		AAA		X02	C4				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	555	**90**	X01	2249				
		Byte		AAA		555		AAA		X02	49				
	Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	555	**90**	(SA) X02	XX00 XX01				
		Byte		AAA		555		AAA		(SA) X04	00 01				
CFI Query (Note 10)		Word	1	55	98										
		Byte		AA											
Program		Word	4	555	AA	2AA	55	555	**A0**	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	**20**						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 11)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 12)			2	XXX	90	XXX	F0								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	**10**
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	**30**
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 13)			1	XXX	**B0**										
Erase Resume (Note 14)			1	XXX	**30**										

Legend

X = Don't care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A19–A12 uniquely select any sector.

Notes

1. See Table 7.1 on page 11 for description of bus operations.
2. All values are in hexadecimal.
3. Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.
4. Data bits DQ15–DQ8 are don't cares for unlock and command cycles.
5. Address bits A19–A11 are don't cares for unlock and command cycles, unless SA or PA required.
6. No unlock or command cycles required when reading array data.
7. The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).
8. The fourth cycle of the autoselect command sequence is a read cycle.
9. The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.
10.Command is valid when device is ready to read array data or when device is in autoselect mode.
11. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
12. The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode. F0 is also acceptable.
13. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
14. The Erase Resume command is valid only during the Erase Suspend mode.

11. Write Operation Status

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 11.1 on page 38 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

11.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 250ns, then the device returns to reading array data.

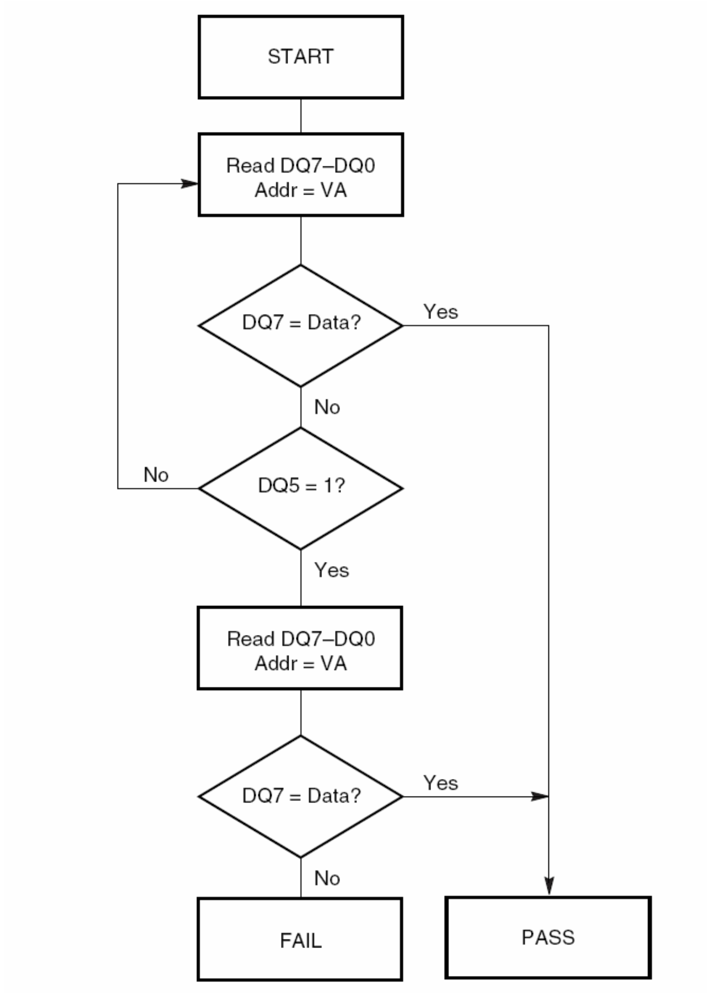
During the Embedded Erase algorithm, Data# Polling produces a *0* on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a *1* on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to *1*; prior to this, the device outputs the *complement*, or *0*. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 1.8 μs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7– DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Figure 17.8 on page 51, illustrates this.

Table 11.1 on page 38 shows the outputs for Data# Polling on DQ7. Figure 11.1 on page 34 shows the Data# Polling algorithm.

Figure 11.1 Data# Polling Algorithm



Notes

1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for
erasure. During chip erase, a valid address is any non-protected sector address.

2. DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.

11.2 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 11.1 on page 38 shows the outputs for RY/BY#. Figures Figure 17.1 on page 45, Figure 17.2 on page 46, Figure 17.5 on page 49 and Figure 17.6 on page 50 shows RY/BY# for read, reset, program, and erase operations, respectively.

11.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. (The system may use either OE# or CE# to control the read cycles.) When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 1.8 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see *DQ7: Data# Polling* on page 33).

If a program address falls within a protected sector, DQ6 toggles for approximately 250 ns after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 11.1 on page 38 shows the outputs for Toggle Bit I on DQ6. Figure 11.2 on page 37 shows the toggle bit algorithm in flowchart form, and *Reading Toggle Bits DQ6/DQ2* on page 36 explains the algorithm. Figure 17.9 on page 51 shows the toggle bit timing diagrams. Figure 17.10 on page 52 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on *DQ2: Toggle Bit II* on page 36.

11.4 DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 11.1 on page 38 to compare outputs for DQ2 and DQ6.

Figure 11.2 on page 37 shows the toggle bit algorithm in flowchart form, and the section *Reading Toggle Bits DQ6/DQ2* on page 36 explains the algorithm. See also the *DQ6: Toggle Bit I* on page 35 subsection. Figure 17.9 on page 51 shows the toggle bit timing diagram. Figure 17.10 on page 52 shows the differences between DQ2 and DQ6 in graphical form.

11.5 Reading Toggle Bits DQ6/DQ2

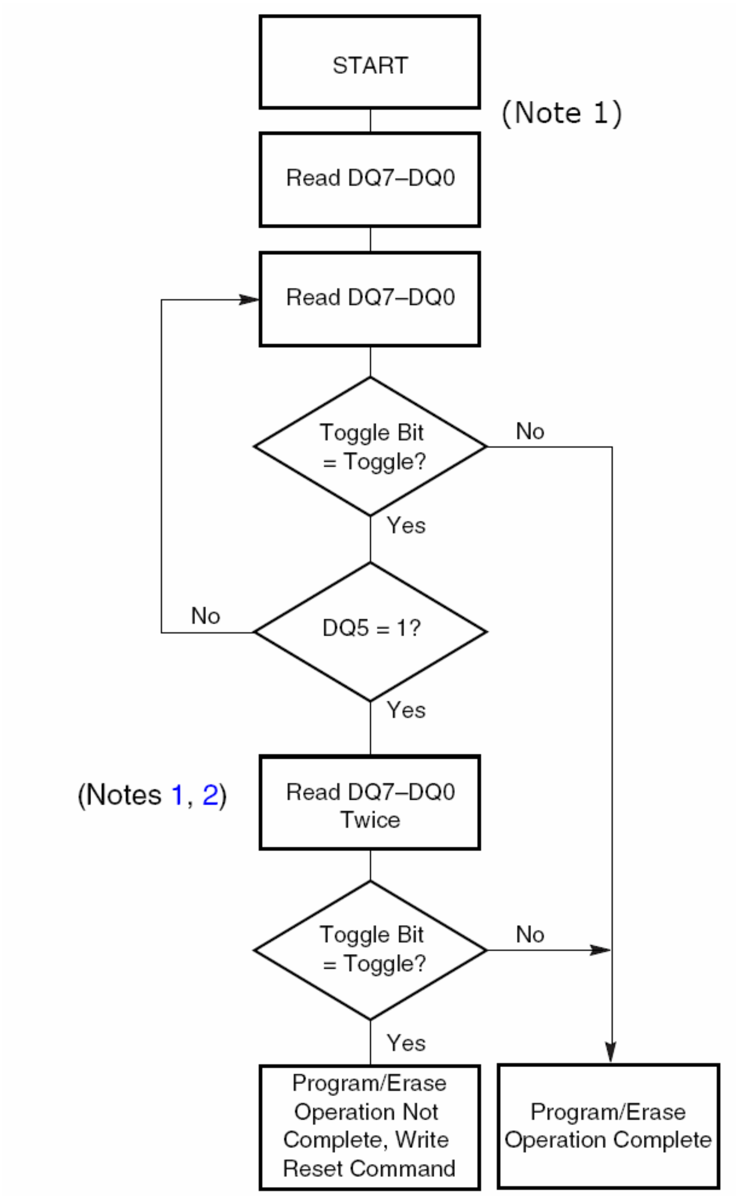
Refer to Figure 11.2 on page 37 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and

DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 11.2 on page 37).

Figure 11.2 Toggle Bit Algorithm



Notes

1. Read toggle bit twice to determine whether or not it is toggling. See text.

2. Recheck toggle bit because it may stop toggling as DQ5 changes to 1. See text.

11.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a *1*. This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a *1* to a location that is previously programmed to *0*. **Only an erase operation can change a *0* back to a *1*.** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a *1*.

Under both these conditions, the system must issue the reset command to return the device to reading array data.

11.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from *0* to *1*. The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 µs. See also *Sector Erase Command Sequence* on page 29.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is *1*, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *0*, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 11.1 shows the outputs for DQ3.

Table 11.1 Write Operation Status

Operation		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes

1. DQ5 switches to 1 *when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See DQ5: Exceeded Timing Limits on page 38 for more information.*

2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

12. Absolute Maximum Ratings

Storage Temperature Plastic Packages	-65℃ to + 150℃
Ambient Temperature with Power Applied	-65℃ to + 125℃
Voltage with Respect to Ground	
V_{CC} (Note 1)	-0.5 V to +4.0 V
A9, OE#, and RESET# (Note 2)	-0.5 V to +12.5 V
All other pins (Note 1)	-0.5 V to V_{CC} +0.5 V
Output Short Circuit Current (Note 3)	200 mA

Notes

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} *to –2.0 V for periods of up to 20 ns. See Figure 13.1 on page 40. Maximum DC voltage on input or I/O pins is* V_{CC} *+0.5 V. During voltage transitions, input or I/ O pins may overshoot to* V_{CC} *+2.0 V for periods up to 20 ns. See Figure 13.2 on page 40.*

2. Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} *to –2.0 V for periods of up to 20 ns. See Figure 13.1 on page 40. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*

3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

4. Stresses above those listed under Absolute Maximum Ratings *may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

13. Operating Ranges

Commercial (C) Devices
Ambient Temperature (TA) 0°C to +70°C

Industrial (I) Devices
Ambient Temperature (TA) -40°C to +85°C

Vcc Supply Voltages
Vcc for standard voltage range 2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Figure 13.1 Maximum Negative Overshoot Waveform

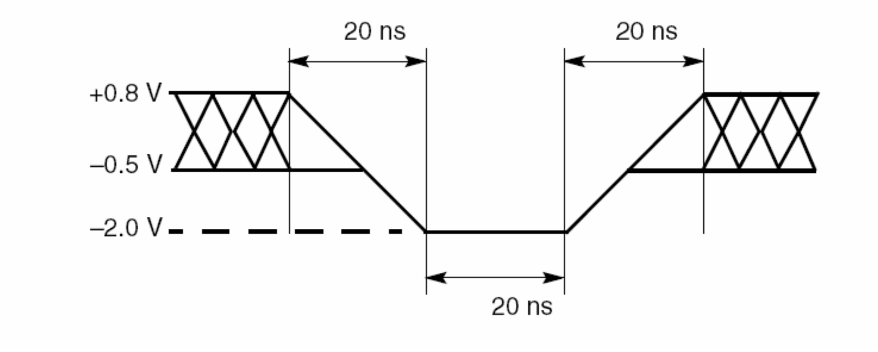
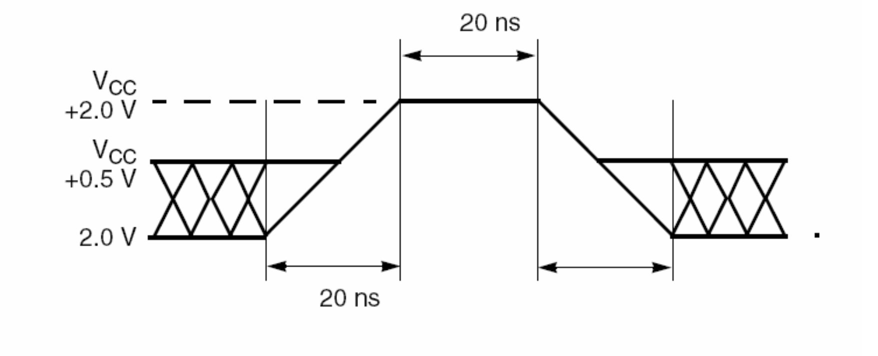


Figure 13.2 Maximum Positive Overshoot Waveform



14. DC Characteristics

14.1 CMOS Compatible

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to $V_{CC,}$ V_{CC} = $V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	V_{CC} = $V_{CC\ max}$; A9 = 12.5V				35	
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to $V_{CC,}$ V_{CC} = $V_{CC\ max}$				±1.0	
I_{CC1}	V_{CC} Active Read Current (Notes 1,2)	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	10MHz		15	30	mA
			5MHz		9	16	
			1MHZ		2	4	
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	10MHz		18	35	
			5MHz		9	16	
			1MHZ		2	4	
I_{CC2}	V_{CC} Active Write Current (Note 2, 3, 4)	CE# = V_{IL}, OE# = V_{IH}			20	35	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET# = V_{CC}±0.3 V			10	50	µA
I_{CC4}	V_{CC} Standby Current During Reset (Note 2)	RESET# = V_{SS}±0.3 V			10		µA
I_{CC5}	Automatic Sleep Mode (Note 2, 5)	V_{IH} = V_{CC}±0.3 V; V_{IL} = V_{SS}±0.3 V			10		µA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} +0.3	
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3 V		11.5		12.5	
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, V_{CC} = $V_{CC\ min}$				0.45	
V_{OH1}	Output High Voltage	I_{OH} = -2.0 mA, V_{CC} = $V_{CC\ min}$		2.4			
V_{OH2}		I_{OH} = -100 µA, V_{CC} = $V_{CC\ min}$		V_{CC}-0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 5)			2.3		2.5	

Notes

1. The ICC current listed is typically less than 2 mA/MHz, with OE# at VIH. Typical V_{CC} is 3.0 V.

2. Maximum ICC specifications are tested with V_{CC} = V_{CC}max.

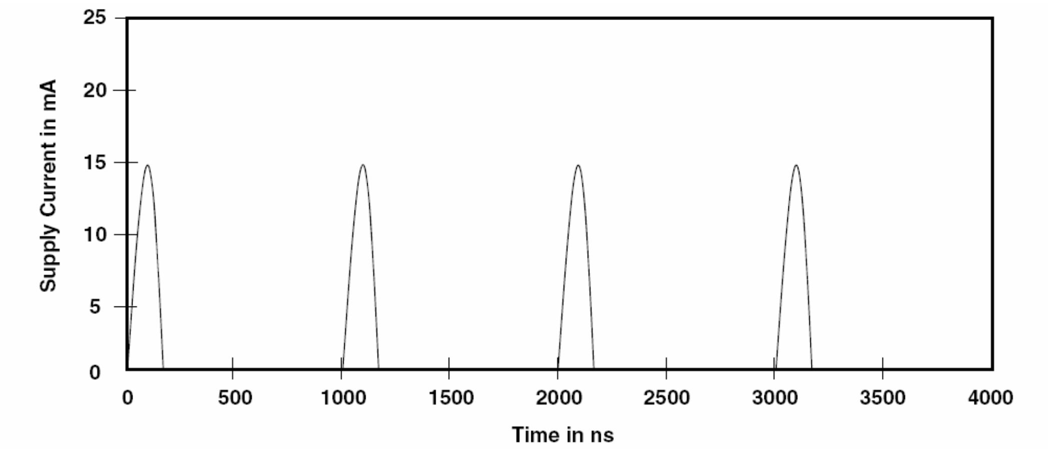
3. ICC active while Embedded Erase or Embedded Program is in progress.

4. Automatic sleep mode enables the low power mode when addresses remain stable for tACC + 30 ns. Typical sleep mode current is 10 uA.

5. Not 100% tested.

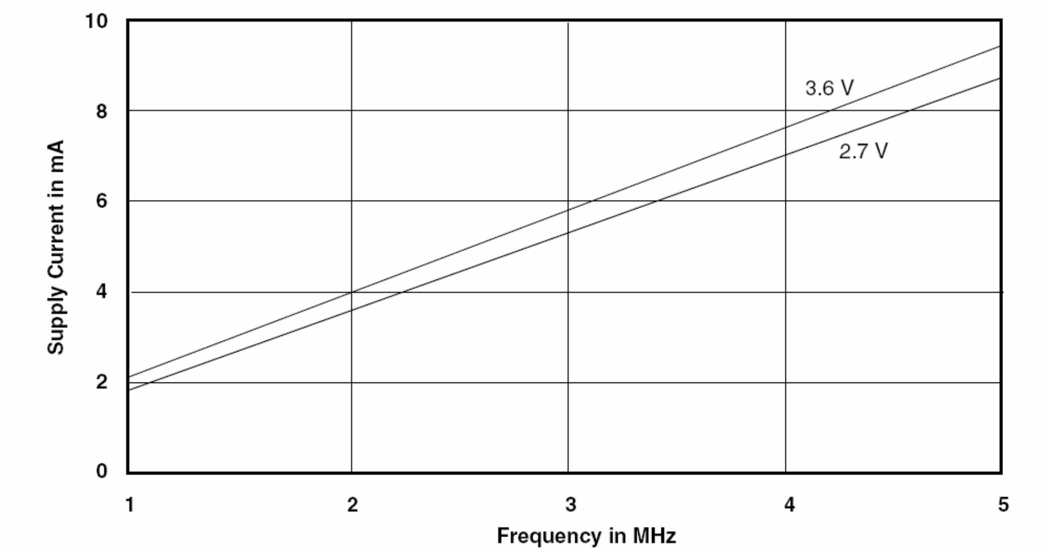
14.2 Zero Power Flash

Figure 14.1 ICC1 Current vs. Time (Showing Active and Automatic Sleep Currents)



Note
Addresses are switching at 1 MHz

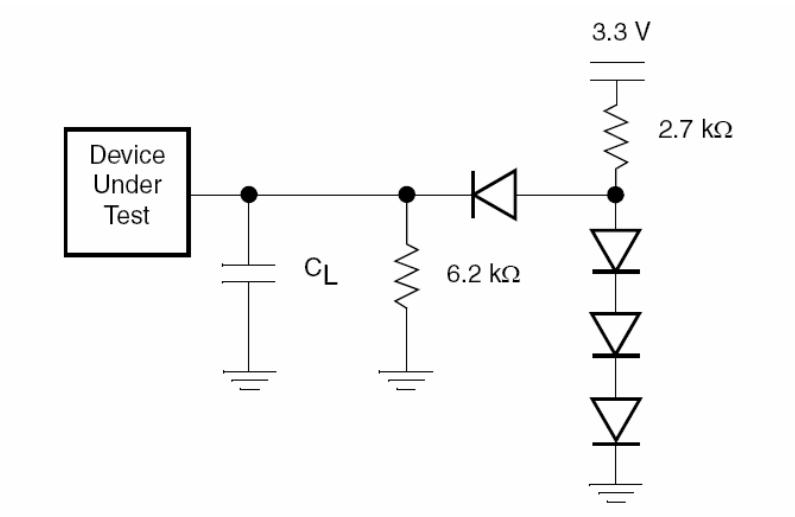
Figure 14.2 Typical ICC1 vs. Frequency



Note
T = 25 °C

15. Test Conditions

Figure 15.1 Test Setup



Note
Diodes are IN3064 or equivalent.

Table 15.1 Test Specification

Test Condition	55R	70	Unit
Output Load	1TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0 or V_{CC}		V
Input timing measurement reference levels	0.5 V_{CC}		
Output timing measurement reference levels	0.5 V_{CC}		

16. Key to Switching Waveforms

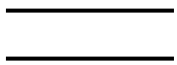
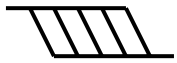
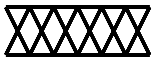
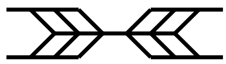
<table>
<tr><th>Waveform</th><th>Inputs</th><th>Outputs</th></tr>
<tr><td></td><td colspan="2">Steady</td></tr>
<tr><td></td><td colspan="2">Changing from H to L</td></tr>
<tr><td></td><td>Changing from L to H</td><td></td></tr>
<tr><td></td><td>Don’t Care, Any Change Permitted</td><td>Changing, State Unknown</td></tr>
<tr><td></td><td>Does Not Apply</td><td>Center Line High Impedance State (High Z)</td></tr>
</table>

Figure 16.1 Input Waveforms and Measurement Levels

17. AC Characteristics

17.1 Read Operations

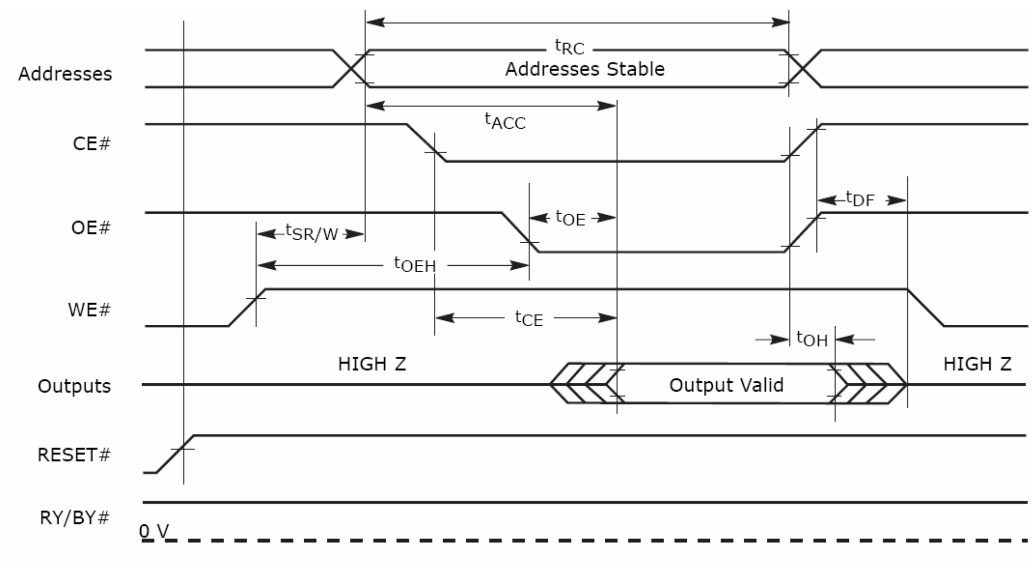
Parameter JEDEC	Parameter Std	Description		Test Setup		Speed Options 55R	Speed Options 70	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	55	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL}	Max	55	70	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	55	70	ns
t_{GLQV}	t_{OE}	Output Enable to Delay		OE# = V_{IL}	Max	25	30	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	16		ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	16		ns
	$t_{SR/W}$	Latency Between Read and Write Operations			Min	20		ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns
t_{AXQX}	t_{OH}	Output Enable Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0		ns

Notes

1. Not 100% tested.

2. See Figure 15.1 on page 43 and Table 15.1 on page 43 for test specifications.

Figure 17.1 Read Operations Timings

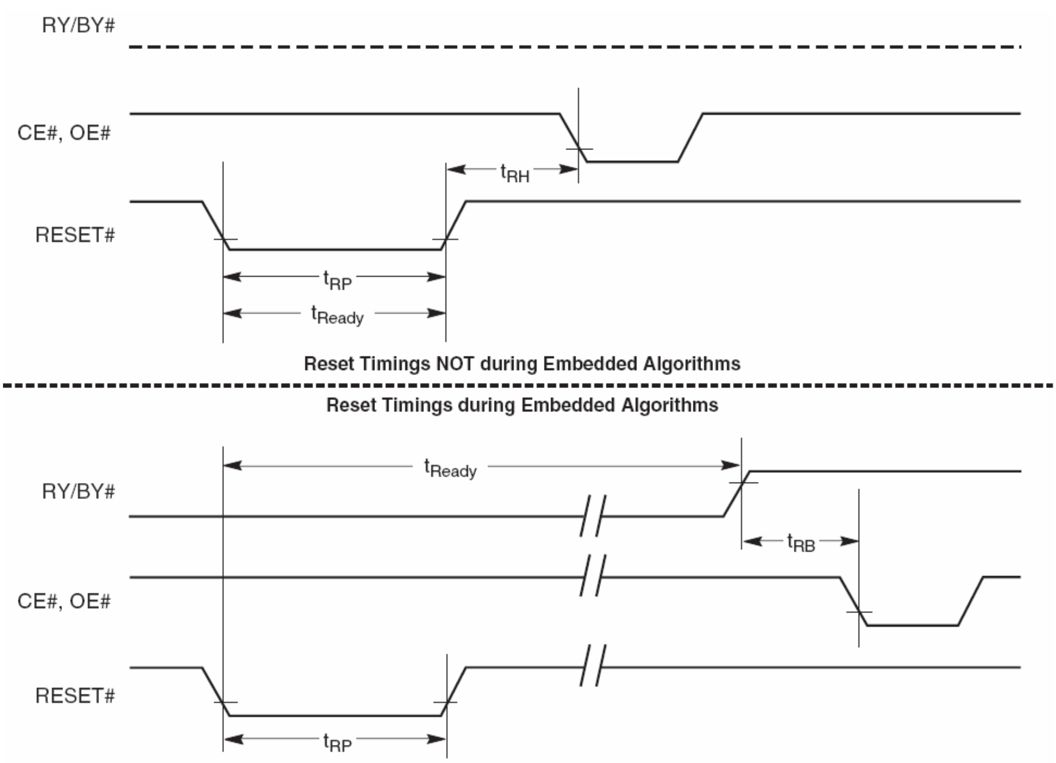


17.2 Hardware Reset (RESET#)

Parameter		Description	Test Setup	All Speed Options	Unit
JEDEC	Std				
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)	Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note
Not 100% tested.

Figure 17.2 RESET# Timings



17.3 Word/Byte Configuration (BYTE#)

Parameter		Description		Speed Options		Unit
JEDEC	Std			55R	70	
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max	5		ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	16		
	t_{FHQV}	BYTE# Switching High to Output Active	Min	55	70	

Figure 17.3 BYTE# Timings for Read Operations

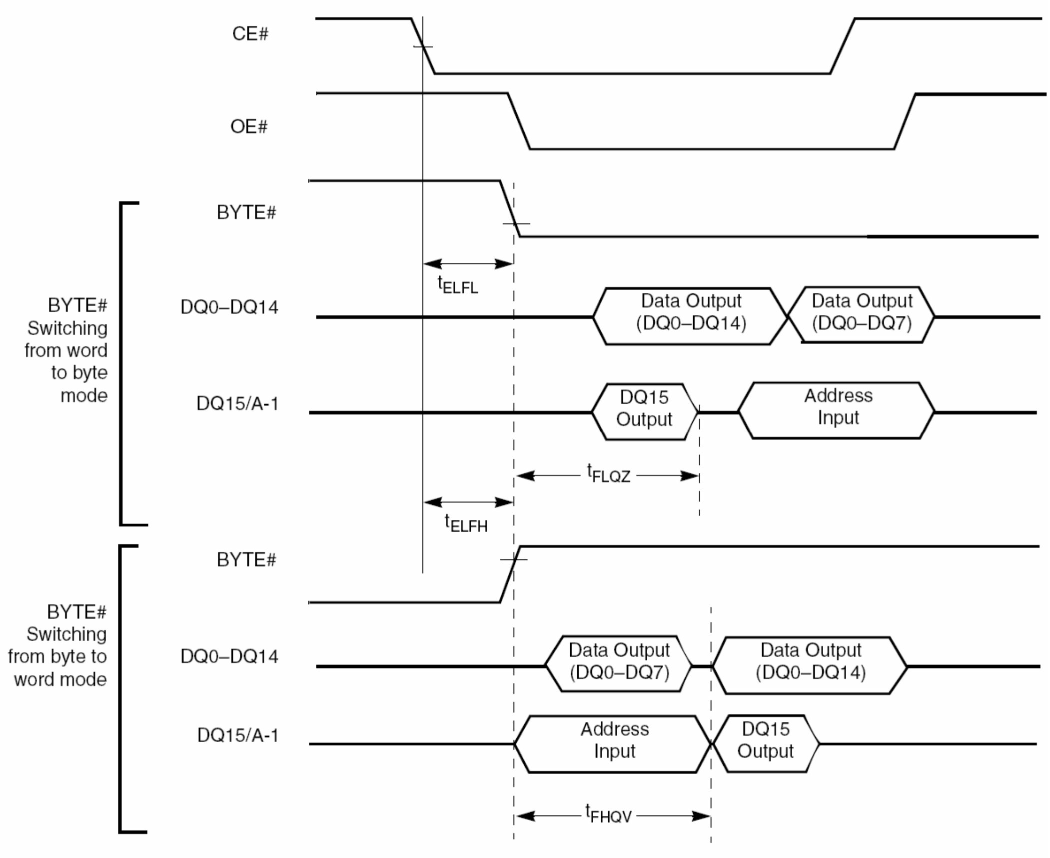
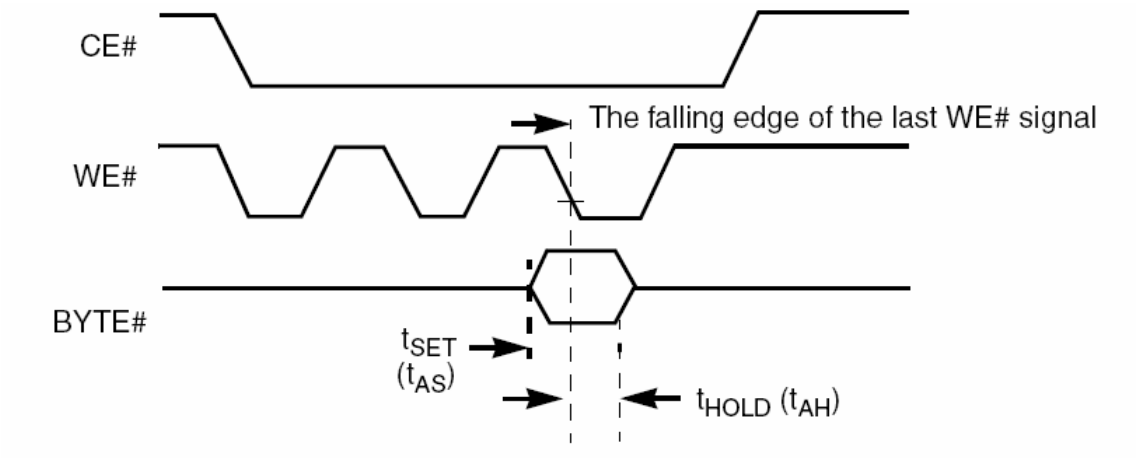


Figure 17.4 BYTE# Timings for Write Operations



Note

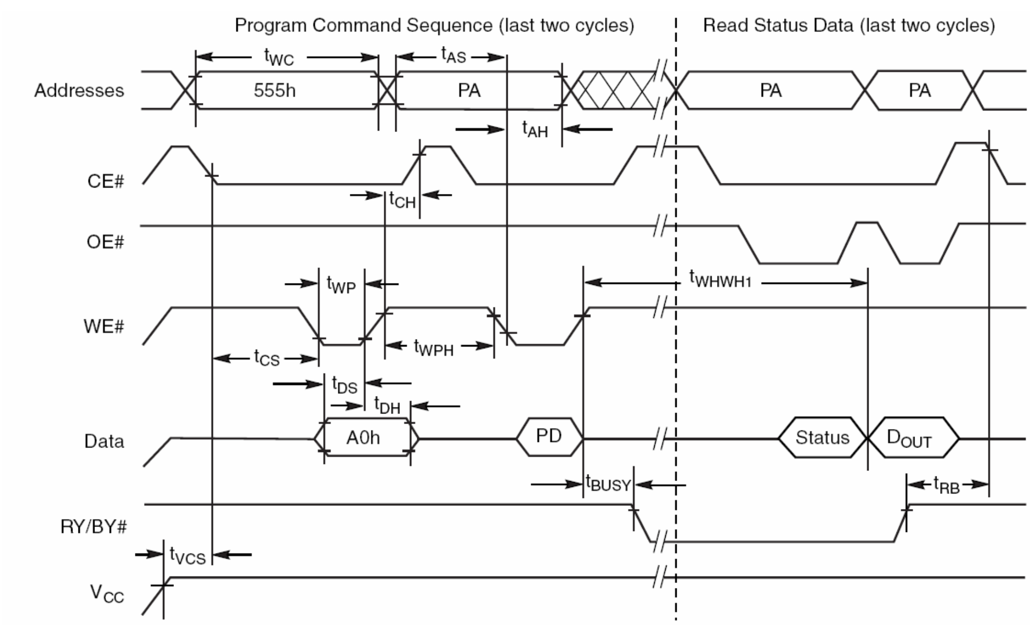
Refer to the Erase/Program Operations table for tAS and tAH specifications.

17.4 Erase/Program Operations

Parameter		Description			Speed Options		Unit
JEDEC	Std				55R	70	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	55	70	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	35	40	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	40	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	25	30	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	25	30	ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	20		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	5		µs
			Word	Typ	7		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.4		sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50		µs
	t_{RB}	Recovery Time from RY/BY#			0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Max	90		ns

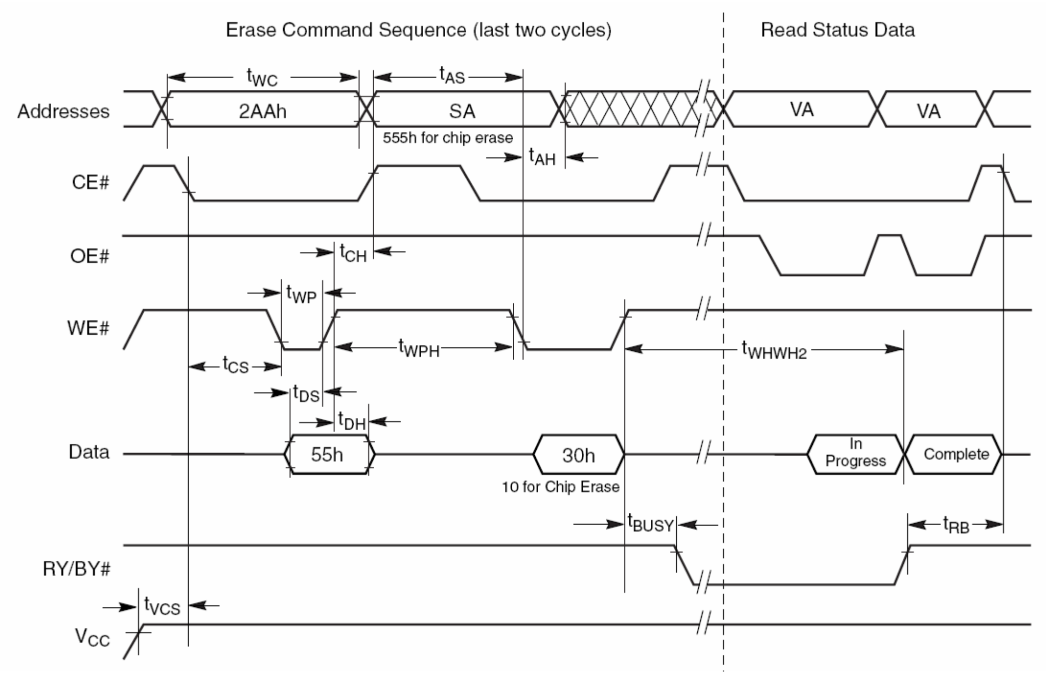
Notes
1. Not 100% tested.
2. See Erase and Programming Performance on page 55 for more information.

Figure 17.5 Program Operation Timings



Notes
1. PA = program address, PD = program data, DOUT is the true data at the program address.
2. Illustration shows device in word mode.

Figure 17.6 Chip/Sector Erase Operation Timings



Notes
1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Write Operation Status on page 13).
2. Illustration shows device in word mode.

Figure 17.7 Back to Back Read/Write Cycle Timing

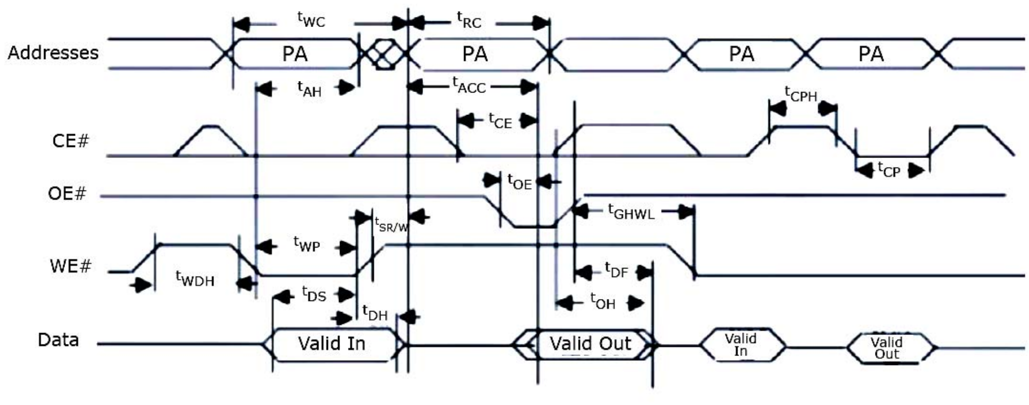
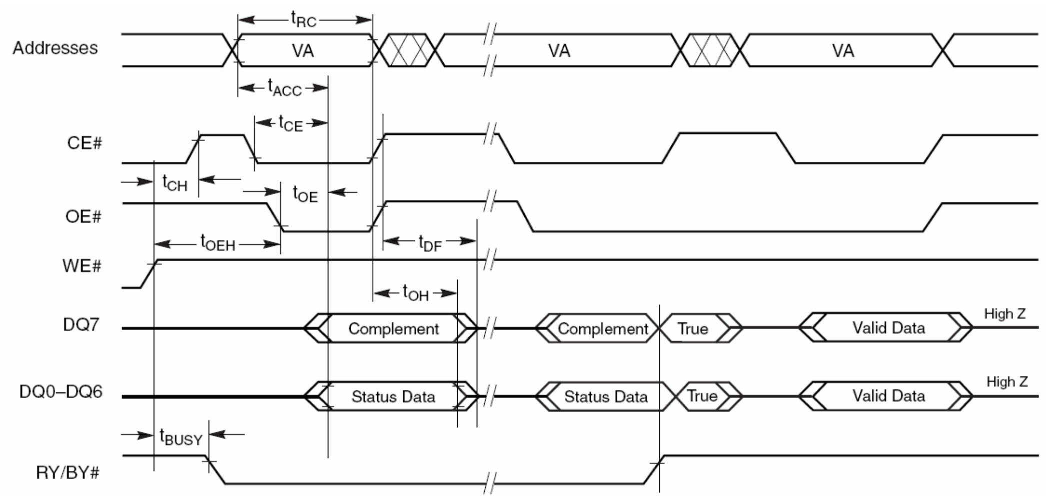
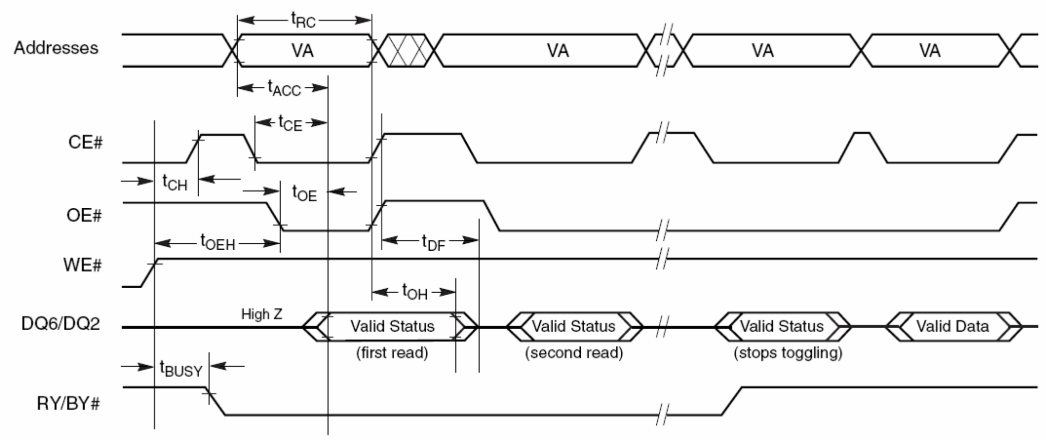


Figure 17.8 Data# Polling Timings (During Embedded Algorithms)



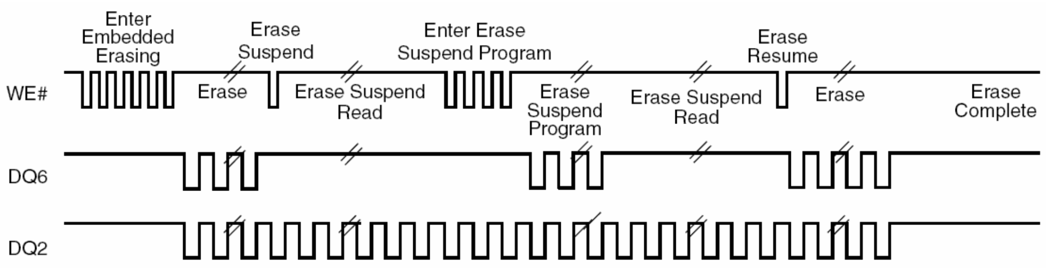
Note
VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 17.9 Toggle Bit Timings (During Embedded Algorithms)



Note
VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 17.10 DQ2 vs. DQ6 for Erase and Erase Suspend Operations



Note
The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.

17.5 Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note
Not 100% tested.

Figure 17.11 Temporary Sector Unprotect/Timing Diagram

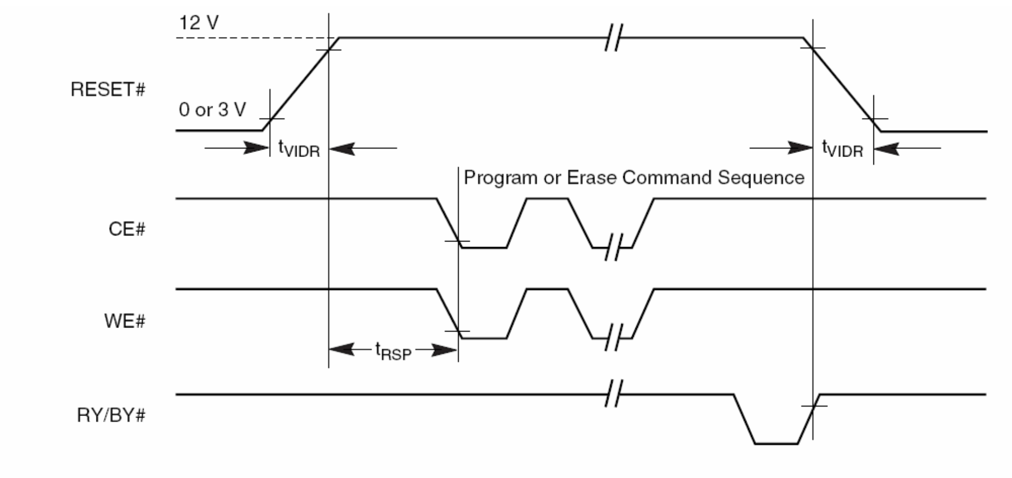
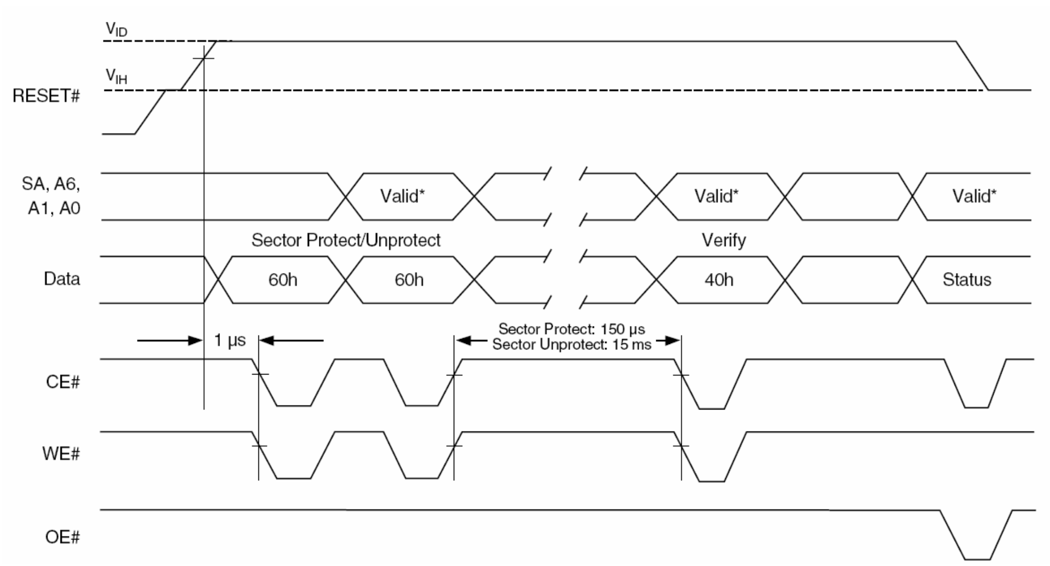


Figure 17.12 Sector Protect/Unprotect Timing Diagram



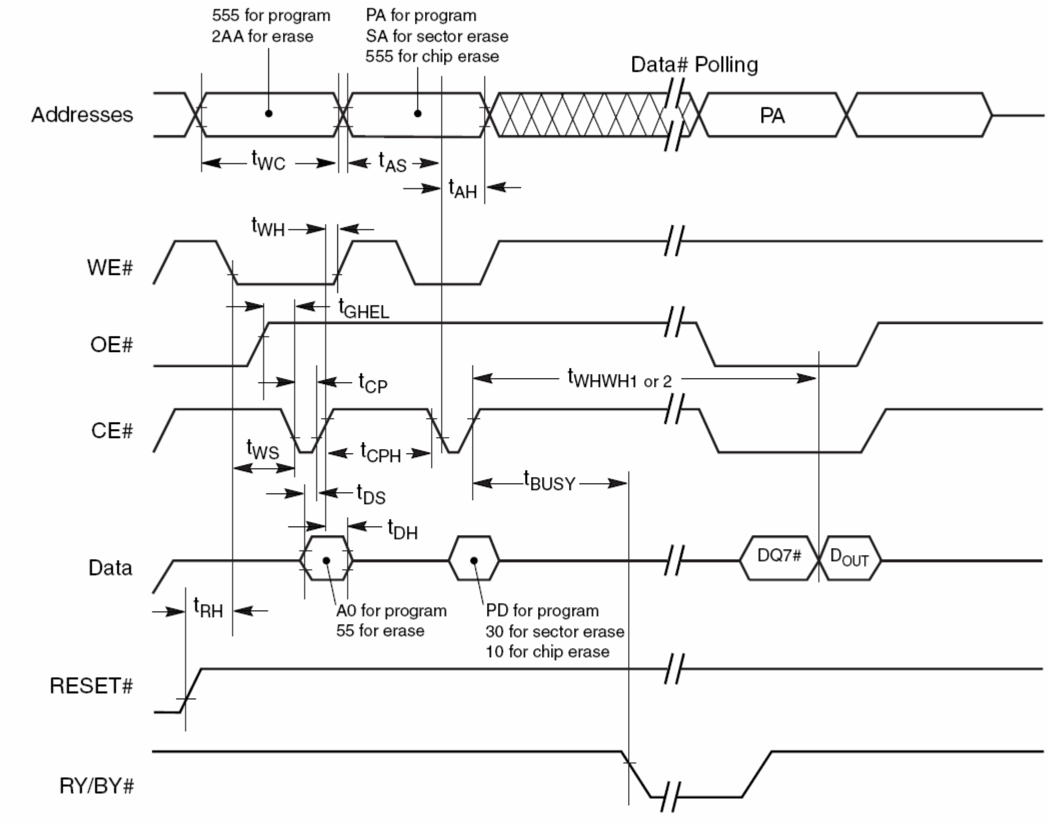
Note
For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.

17.6 Alternate CE# Controlled Erase/Program

Parameter					**Speed Options**		
JEDEC	**Std**	**Description**			**55R**	**70**	**Unit**
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	55	70	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	35	40	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	40	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35		ns
t_{EHEL}	t_{CPH}	CE# Pulse Width		Min	30		ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	20		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	5		µs
			Word	Typ	7		
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.4		sec

Notes
1. Not 100% tested.
2. See Erase and Programming Performance on page 55 for more information.

Figure 17.13 Alternate CE# Controlled Write Operation Timings



Notes

1. PA = program address, PD = program data, DQ7# = complement of the data written to the device, DOUT = data written to the device.

2. Figure indicates the last two bus cycles of the command sequence.

3. Word mode address used as an example.

18. Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.4	10	s	
Chip Erase Time		13		s	
Byte Programming Time		5	150	µs	Excludes system level Overhead (Note 4)
Word Programming Time		7	210	µs	
Chip Programming Time (Note 3)	Byte Mode	13	38	s	
	Word Mode	9	26	s	

Notes
1. Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0 V, 100,000 cycles, checkerboard data pattern.
2. Under worst case conditions of 90°C, V_{CC} = 2.7 V, 100,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.
4. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 10.1 on page 32 for further information on command definitions.
5. The device has a minimum erase and program cycle endurance of 100,000 cycles per sector.

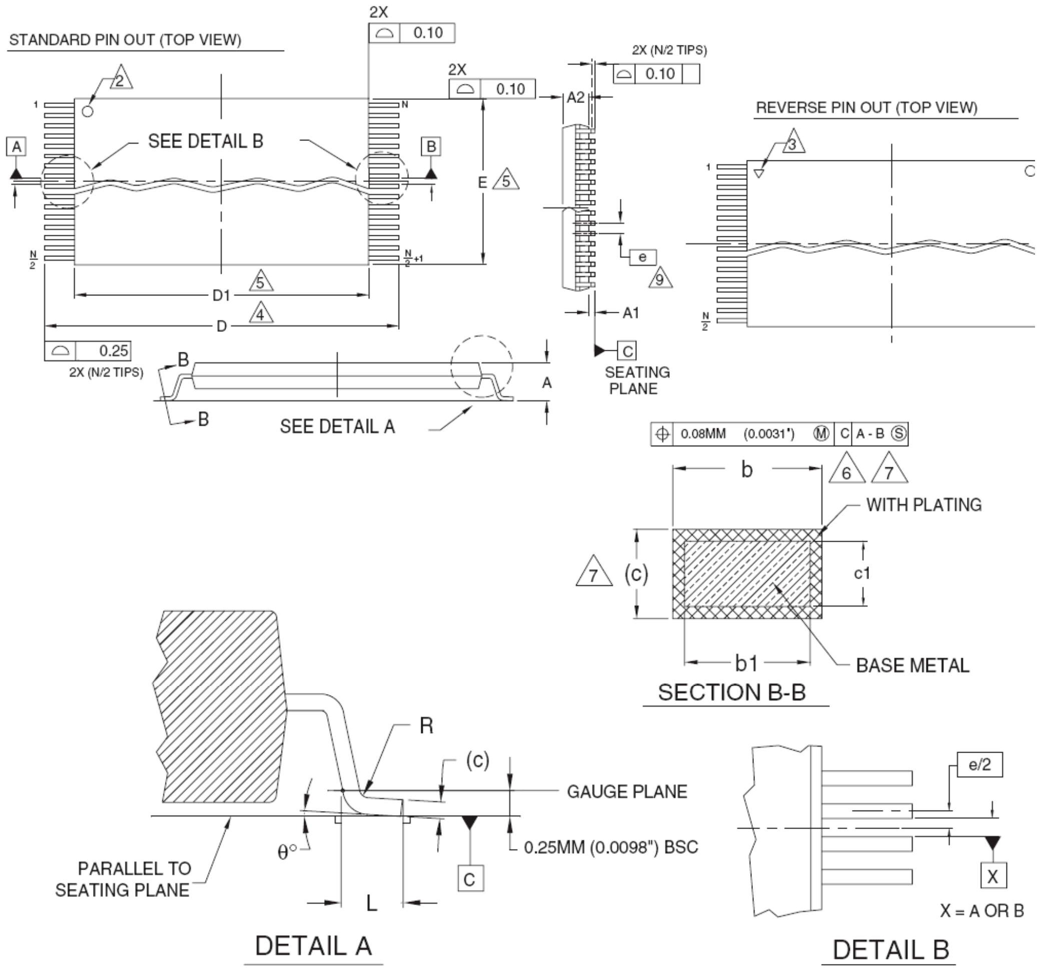
19. TSOP and BGA Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	Package	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
			BGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
			BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF
			BGA	3.9	4.7	pF

Notes
1. Sampled, not 100% tested.
2. Test conditions TA = 25°C, f = 1.0 MHz.

20. Physical Dimensions

20.1 TS048 48-Pin Standard TSOP



Jedec	MO-142 (D) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8°
R	0.08	—	0.20
N	48		

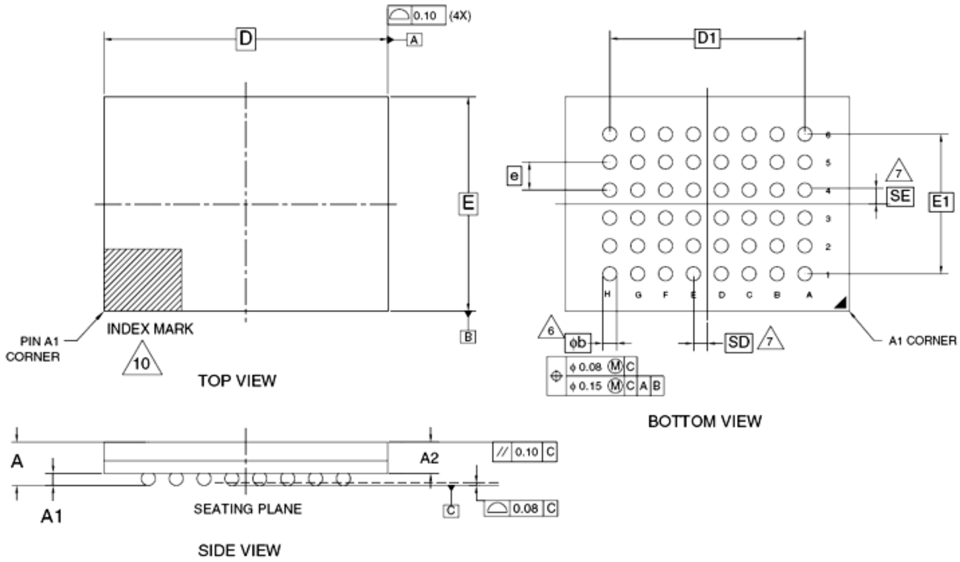
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

Note

For reference only. BSC is an ANSI standard for Basic Space Centering.

20.2 —48-Ball Fine-Pitch Ball Grid Array (FBGA) 6.00 mm x 8.00 mm



PACKAGE	VBK 048			
JEDEC	N/A			
	8.00 mm x 6.00 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.10	OVERALL THICKNESS
A1	0.21	---	---	BALL HEIGHT
A2	0.7	---	0.82	BODY THICKNESS
D		8.00 BSC.		BODY SIZE
E		6.00 BSC.		BODY SIZE
D1		5.60 BSC.		BALL FOOTPRINT
E1		4.00 BSC.		BALL FOOTPRINT
MD		8		ROW MATRIX SIZE D DIRECTION
ME		6		ROW MATRIX SIZE E DIRECTION
N		48		TOTAL BALL COUNT
φb	0.30	---	0.40	BALL DIAMETER
e		0.80 BSC.		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		---		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

Additional Features (ES29LV160F)

In ES29LV160F device, a few of additional and useful features are provided. These are additional so that its functionality is 100% compatible with other flash devices. More explanations for each additional features or functions are described in detail below.

- Deep power-down mode (less than 1uA)
- Program acceleration mode (ACC pin)
- Page buffer program (32 words)
- 256 bytes of security sector for customer codes
- Factory and customer-lockable functions for the security sector

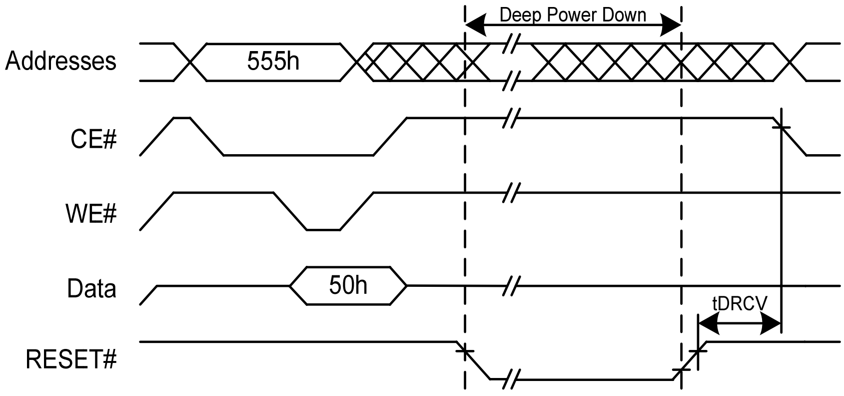
A1. Deep power-down mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is reduced, and the outputs are placed in the high impedance state, independent of the OE# input. The device normally enters the CMOS standby mode (typically 10uA) when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V.

In ES29LV160F device, another power-saving mode is provided, called '**deep power-down mode'**. The device can be placed into this deep power-down mode by issuing a command. And then RESET# should be taken to VIL (Vss±0.3V) to fully suppress the current consumption down to less than typically 1uA(maximum 10uA). In other word, the extremely low current consumption can be kept only while RESET# is held at Vss±0.3V.

As soon as RESET# goes to High (VIH), the device returns to normal read mode. But, a period of recovery time (Min. tDRCV is 20usec) is needed before the device is fully ready to read the data from the cell array with normal fast access time. Refer to the command cycles to enter the **deep power-down mode** at the table A1.

Fig. A1 Deep Power Down mode



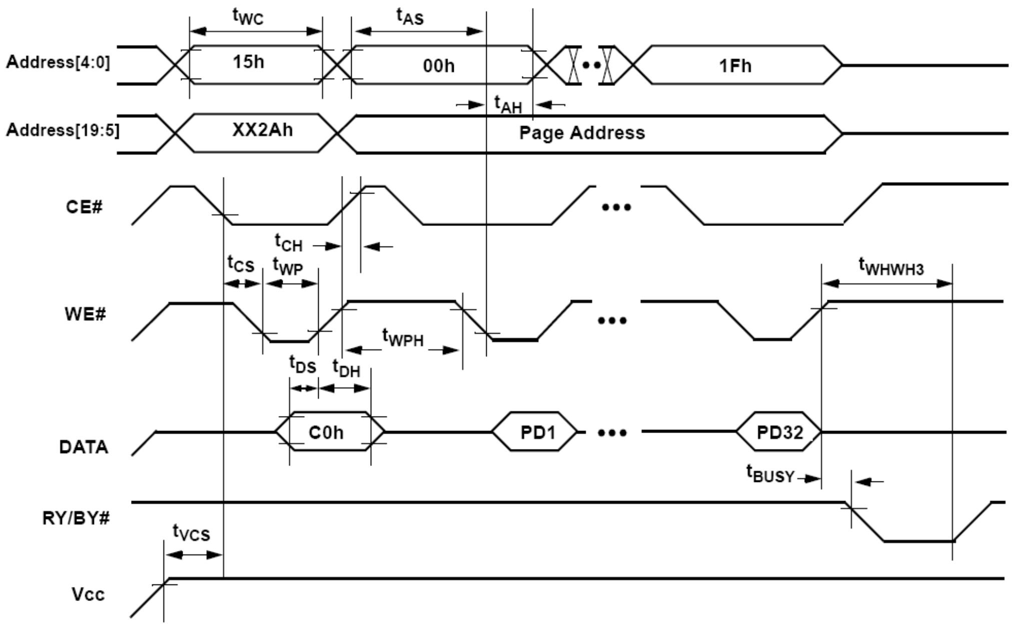
A2. Page Program

In ES29LV160F device, a page program is provided for more accelerated programming operation. In this mode, 32 words are parallel programmed to greatly reduce total program time. If this mode is combined with ACC (12V), even faster program result can be obtained. As shown in the program performance table A2, total program time can be reduced down to **30%** at maximum, compared with normal program mode..

Page Programming allows the system to write 32 words (BYTE#=High) in one period of programming operation. This results in faster and more effective programming time than the standard programming algorithms. The page program command sequence is initiated by writing two unlock write cycles, followed by the page program set-up command. And then full number (32 cycles) of address/data cycles should be sequentially followed to activate the page program operation. The actual page program starts at the rising edge of the last WE# pulse of the total required address/data loading cycles.

One after a page program is started; the system is not required to provide further controls or timings. During a page program operation, data toggle (DQ6) should be used for check if the page program operation is completed or not, instead of DQ7. Data polling by DQ7 is not supported during the page program operation. It should be also noted that if the Address [4:0] are not written either sequentially or written completely to the last address, some data may be over-written, lost or not guaranteed properly. Moreover, Address [19:5] should not be changed until page program starts.

Fig. A2 Page program operation



A3. Additional Commands Set

Table A1. Additional Command Definitions

Command Sequence			Cycles	Bus Cycles									
				First		Second		Third		Fourth		Last	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Auto Select	Security Sector Protection	Word	4	555	AA	2AA	55	555	90	X03	82/02/42 (Note 1)		
		Byte		AAA		555		AAA		X06			
	Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA)X02	00/01 (Note2)		
		Byte		AAA		555		AAA		(SA)X04			
Deep Power-down		Word	3	555	AA	2AA	55	555	50				
		Byte		AAA		555		AAA					
Page Program (Note3)		Word	35	555	AA	2AA	55	555	C0	PA1	PD1	PA32	PD32
Enter Security Sector		Word	3	555	AA	2AA	55	555	88				
		Byte		AAA		555		AAA					
Exit Security Sector		Word	4	555	AA	2AA	55	555	90	XXX	00		
		Byte		AAA		555		AAA					

X = Don't Care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed.
PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A19-A12 uniquely select any sector. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

Note 1) Data 82h (Factory-locked), 02h (Customer-lockable), and 42h (Customer-locked)
Note 2) Data 00h (for an unprotected sector), 01h (for a protected sector)
Note 3) Page Program is supported only at Word Mode

A4. Program Acceleration Mode (ACC pin)

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory. Programming speed can be highly accelerated during this mode. Furthermore, **Unlock bypass mode** is automatically activated in this mode (when 12V is applied to ACC pin). Approximately 40% program time can be saved with this mode If the system asserts VHH (11.5V~12.5V) on this pin, the device automatically enters Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. Only two-cycle program command sequences are required because the unlock bypass mode is automatically activated in this acceleration mode. The device returns to the normal operation when VHH is removed from the ACC pin. It should be noted that the ACC pin must not be at VHH for operations other than accelerated programming, or device damage may result.

.ACC pin is an extra pin to be used for the accelerated programming operation. However, in case that users do not want this pin, the ACC pin can be **floated** or dealt as 'No Connection (NC)'. This unique feature of flexible pin connectivity provides easier compatibility and flexibility to a lot of different users under different system environments.

Table A2. Page program and ACC acceleration program performance

Parameter	Typ	Max	Unit	Effective time
Byte Program	5	150	us	
Byte Program with ACC	4	120	us	
Word Program	7	210	us	
Word Program with ACC	4	120	us	
Page Program (t_{WHWH3})	170	510	us	5usec/word
Page Program with ACC	70	210	us	**2usec/word**

Table A3. DC Characteristics for Program Acceleration Mode

Parameter	Description	Test Condition	Min	Max	Unit
I_{HH}	ACC Input Load Current	$V_{CC}=V_{CC\ MAX}$;ACC=12V	5	12	mA
V_{HH}	Voltage for Acceleration	Vcc = 3.3V	11.5	12.5	V

A5. Security Sector (256 bytes)

The security sector of the ES29LV160F device provides an extra flash memory space that enables permanent part identification through an Electronic Serial Number (ESN). The security sector uses a security lock-Indicator Bit (DQ7) to indicate whether or not the security sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning a factory locked part. This ensures the security of the ESN once the product is shipped to the field. Note that the ES29LV160F has a security sector size of 256 bytes.

Security Lock-Indicator Bit (DQ7)

In the device, the security sector can be provided in either factory locked version or customer lockable version. The factory-locked version is always protected when shipped from the factory, and has the security lock-Indicator Bit permanently set to a “1”.
The customer-lockable version is shipped with the security sector unprotected, allowing customers to utilize the sector in any manner they choose. The customer-lockable version has the security lock-Indicator Bit permanently set to a “0”. Thus, the security lock-Indicator Bit prevents customer-lockable devices from being used to replace devices
that are factory locked. The security customer indicator Bit(DQ6) is permanently set to “1” if the part has been customer locked, permanently set to “0” if the part has been factory locked, and is “0” if customer lockable.

Access to the Security Sector

The security sector can be accessed through a command sequence: Enter security and Exit security sector commands. After the system has written the Enter security sector command sequence, it may read the security sector by using the addresses normally occupied by the boot sectors.
This mode of operation continues until the system issues the Exit security sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device returns to read mode in which the normal boot sectors can be accessed, instead of the security sector.

Factory-Locked Device

In a factory-locked device, the security sector is protected when the device is shipped from the factory. The security sector cannot be modified in any way. So, customer own codes like ESN (Electronic Serial Number) can be safely stored in this factory-locked security sector arera.
The device is available preprogrammed with one of the following:

ESN (Electronic Serial Number)

In devices that have an ESN, a Bottom Boot device will have the 16-byte (8-word) ESN in sector 0 at addresses 000000h-00000Fh in byte mode (or 000000h-000007h in word mode). In the Top Boot device the ESN will be in sector 34 at addresses 1FFF00h-1FFF0Fh in byte mode (or FFF80h-FFF87h in word mode).

Factory Code Service of ESI

Customers may opt to have their code programmed by ESI (factory service). A service called ESI ‘special code service’ is provide for customers. ESI (factory) can program the customer’s code, with or without the random ESN, according to the customer request. The devices are then shipped from ESI factory with the Security Sector permanently locked. Contact a ESI representative for details on using ESI Special-Code service.

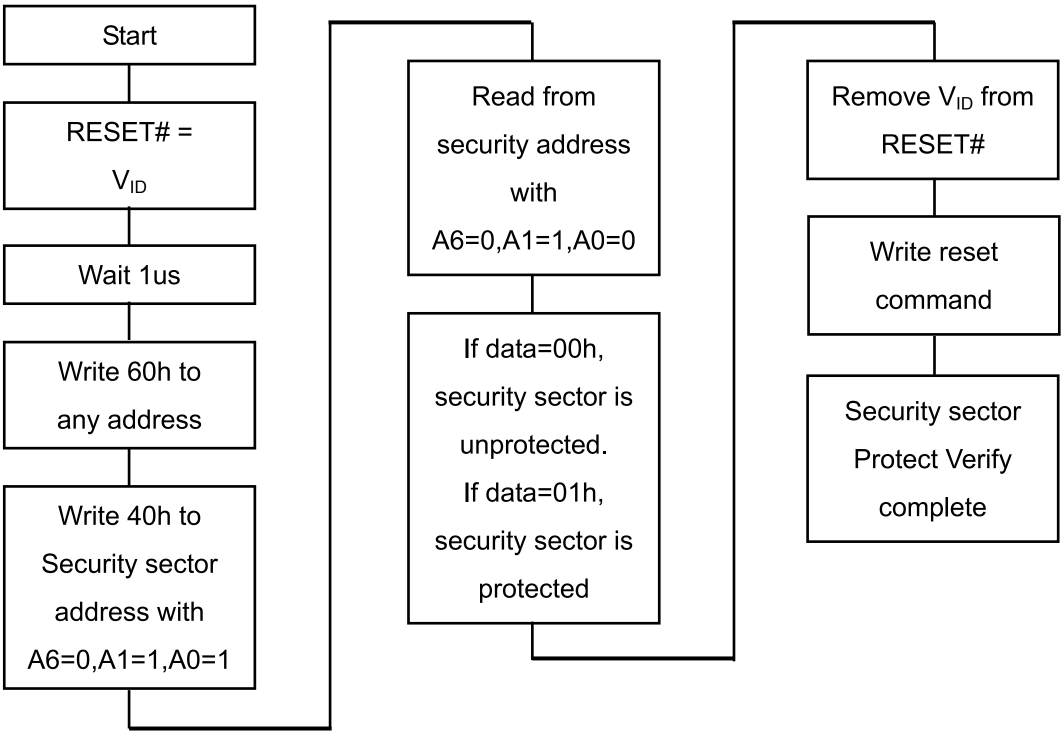
Customer-Lockable Device

The customer lockable version allows the security sector to be freely programmed or erased and then permanently locked. Note that the ES29LV160F has a security sector size of 256 bytes (128 words). Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the security sector.

Protection of the Security Sector

The security sector area can be protected using the following procedures: Write the three-cycle “Enter security sector command” sequence, and then following the in-system sector protect algorithm as shown in Fig. 7.3, This allows In-system protection of the security sector without raising any device pin to a high voltage. To verify the protect/ unprotect status of the security sector, follow the algorithm shown in Fig. A3.

Fig. A3 Security Sector Protection Verify



Exit from the Security Sector

Once the Security Sector is locked protected and verified, the system must write the Exit Security Sector Region command sequence to return to reading and writing the remainder of the array.

Caution for the Security Sector Protection

The security sector protection must be used with caution since, once protected, there is no procedure available for unprotecting the security sector area and none of the bits in the security sector memory space can be modified in any way.

Table A4. Security-lock check by A9 High-voltage method

Description	CE#	OE#	WE#	A9	A6	A1	A0	DQ8~DQ15		DQ7 ~DQ0
								BYTE# = VIH	BYTE# =VIL	
Security Sector Indicator Bit(DQ7)	L	L	H	VID	L	H	H	X	X	82h (Factory Locked), 02h (Unlocked). 42h(Customer Locked)

A6. Manufacturer Code of ESI

Manufacturer code of ESI is 4Ah. This manufacturer code can be easily read out from the device by autoselect command. Once after the device enters the auto-select mode, it can be accessed by one of two ways. Just one read cycle (with A6, A1 and A0 = 0) can be used or four consecutive read cycles (with A6 = 1 and A1, A0 = 0) for continuation code (7Fh) and then another last cycle for (with A6, A1 and A0 = 0) can be used for reading the ESI manufacturer code (4Ah)

Table A5. One-cycle and Five-cycle read for Manufacturer Code (ESI = 4Ah)

Status	Cycles	One-cycle Read		Five-cycle Read	
		Address (Word/Byte)	Data	Address	Data
Autoselect command (3 unlock cycles)	1st	555/AAA	AA	555/AAA	AA
	2nd	2AA/555	55	2AA/555	55
	3rd	555/AAA	90	555/AAA	90
Manufacturer Code Read Cycles	1st	**00**	**4A**	40	7F
	2nd			40	7F
	3rd			40	7F
	4th			40	7F
	5th			**00**	**4A**

A7. Sector protection and un-protection by A9 High-Voltage

The ES29LV160F features hardware sector protection. In the device, sector protection is performed on the sectors. Once after a sector is protected, any program or erase operation is not allowed in the protected sector. The previously protected sectors must be unprotected by one of the unprotect methods provided here before changing data in those sectors.
Sector protection or unprotection can be implemented via two methods.

- **In-system method**
- **A9 High-voltage method**

To check whether the sector protection or unprotection was successfully executed or not, another operation called "verification" needs to be performed after the protection or unprotection operation on a sector. All protection and unprotect verifications provided in the device are summarized in detail at the Table A6.

'A9 High-voltage method', an alternate method intended only for programming equipment, must force VID (11.5~12.5V) on address pin A9 and control pin OE# with A6=0, A1=1 and A0=0. Refer to Fig.A6 and Fig.A7 for timing diagram and Fig.A4 and Fig.A5 for the protection/unproection algorithm.

Table A6. Autoselect code by A9-High Voltage Method

Description	CE#	OE#	WE#	A19 To A12	A9	A6	A1	A0	DQ8~DQ15		DQ7 ~DQ0
									BYTE# = VIH	BYTE# =VIL	
Manufac-tureID:ESI	L	L	H	X	VID	L	L	L	X	X	**4Ah**
Device ID: ES29LV160F	L	L	H	X	VID	L	H	H	22H	X	**C4h(T), 49h(B)**
Sector Protection Verification	L	L	H	SA	VID	L	L	L	X	X	01h(protected) 00h(unprotected)
Security Sector Indicator Bit(DQ7)	L	L	H	X	VID	L	H	H	X	X	82h(Factory Locked) 02h(Unlocked) 42h(Customer Locked)

Note) Other pins are "don't care", and ACC pin can be floated (NC) or connected to V_{CC} or Vss, except an V_{HH} (=12V).

A9 High-Voltage Method

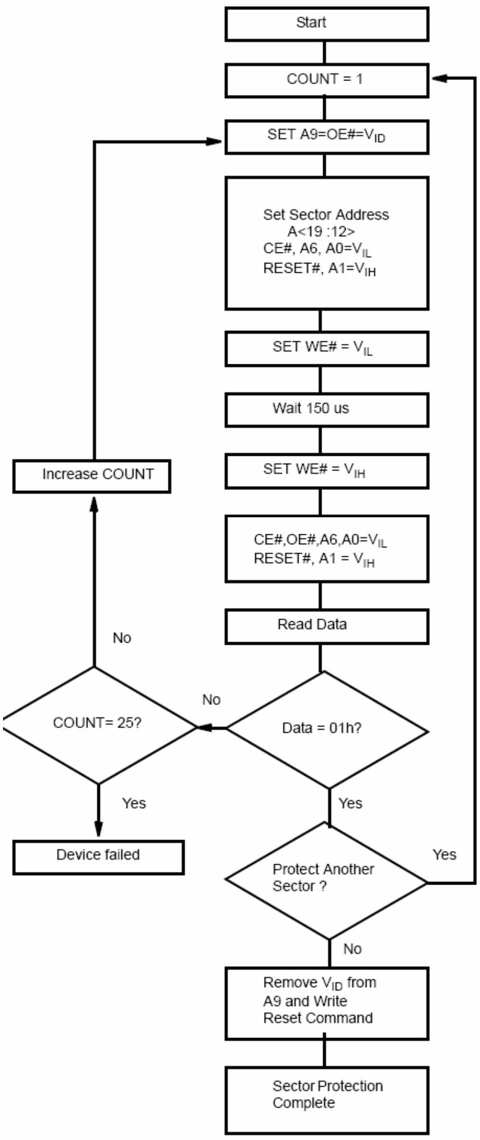


Fig. A4 Sector Protection Algorithm

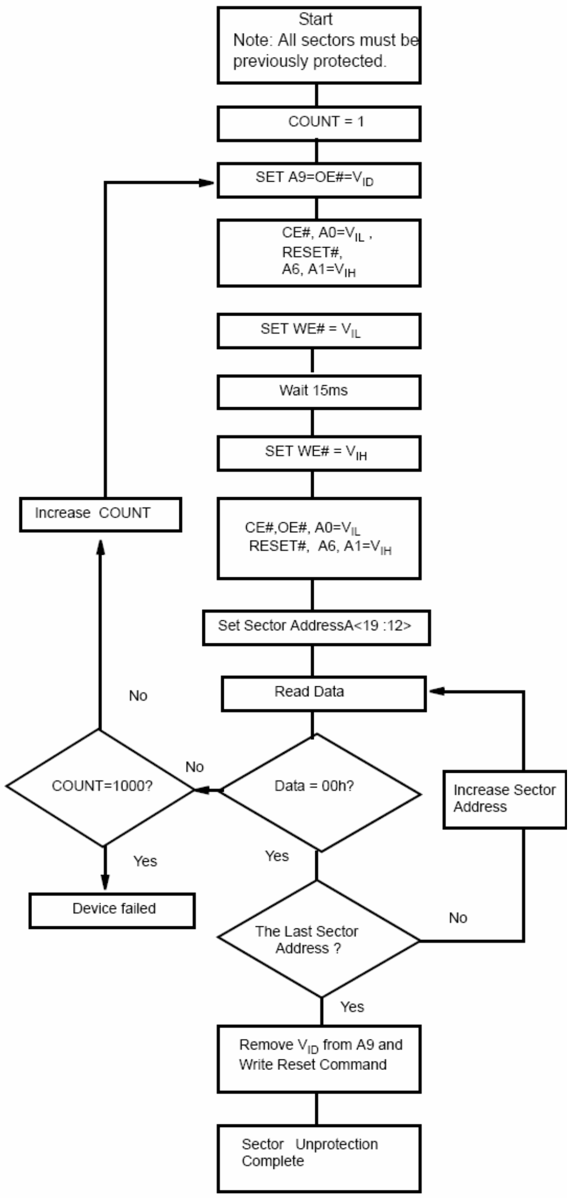


Fig. A5 Sector Unprotection Algorithm

Parameter	Description	Test Setup	Speed Options		Unit
			55R	70	
t_{OE}	Output Enable to Output Delay	Max	25	30	ns
t_{VIDR}	Voltage Transition Time	Min	500		
t_{WPP1}	Write Pulse Width for Protection Operation	Min	150		us
t_{WPP2}	Write Pulse Width for Unprotection Operation	Min	15		ms
t_{OESP}	OE# Setup Time to WE# Active	Min	4		us
t_{CSP}	CE# Setup Time to WE# Active	Min	4		
t_{ST}	Voltage Setup Time	Min	4		

Fig. A6 Sector Protection by A9-High Voltage Method

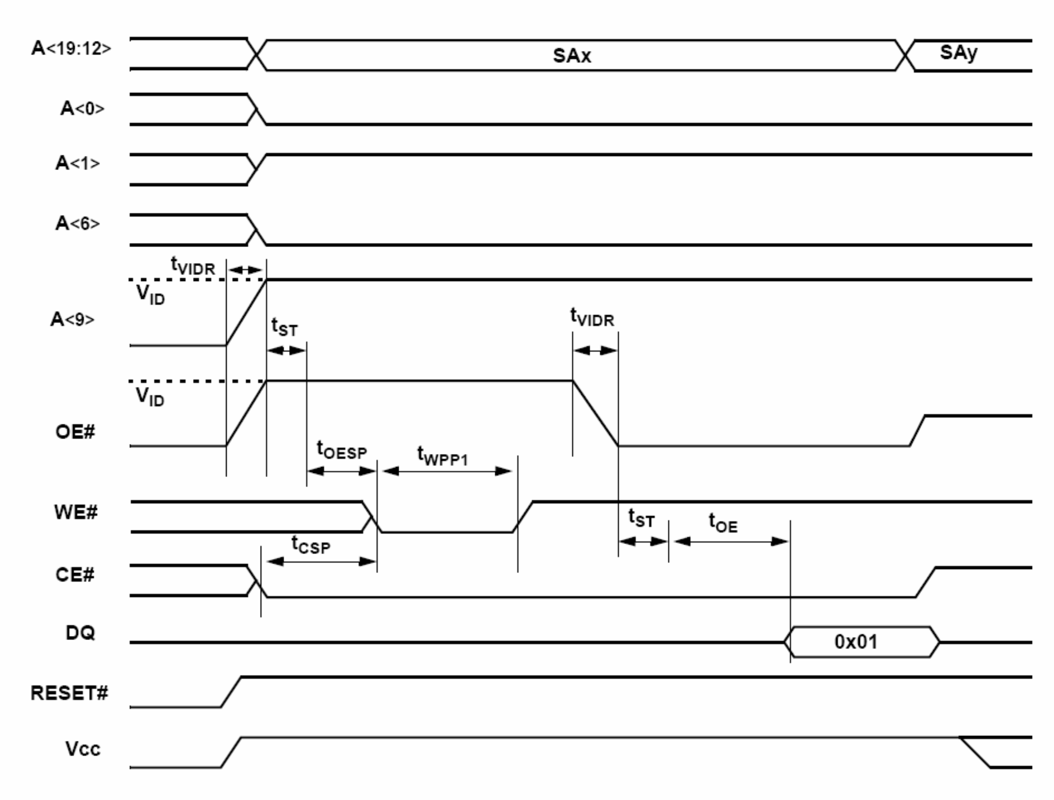
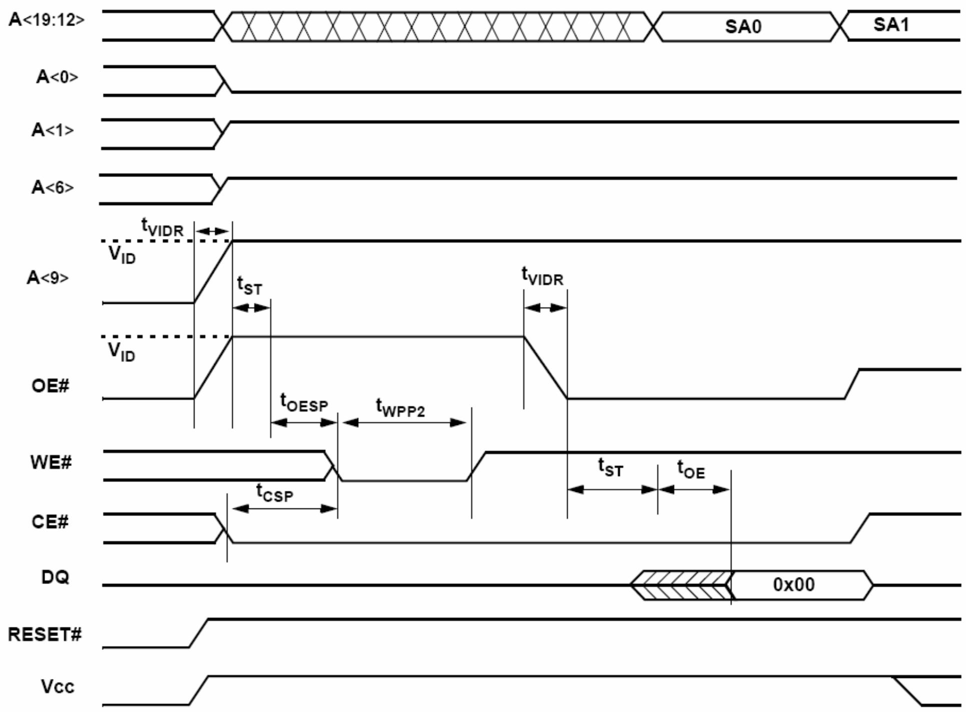


Fig. A7 Sector Unprotection by A9-High Voltage Method



Revision Summary

1. **Revision 0A (Dec 12, 2007)**
   Initial release